

MARRI LAXMAN REDDY INSTITUTE OF TECHNOLOGY AND MANAGEME

Accredited by NBA and NAAC with 'A' Grade & Recognized Under Section2(f) & 12(B)of the UGC act, 1956

II B.Tech I Sem Supplementary Examination, July-2022 Computer Organization and Microprocessor (IT)

Time: 3 Hours.	
N	

Max. Marks: 70

Note: 1. Answer any FIVE questions.

2. Each question carries 14 marks and may have a, b as sub questions.

1	a)	List out the phases for each instruction cycle and show the flowchart for instruction cycle.	7M	C01	BL-1
	b)		7M	C01	BL-2
2		Define control memory and micro programmed control unit. Outline and inspect the block diagram of a control memory and the associated hardware needed for selecting the next microinstruction address.		CO1	BL-2
3		Label the flag register of 8086 and examine the information represented by each flag.	7M	C02	BL-4
	b)	Illustrate the architecture of the 8086 processor with a neat diagram.	7M	CO2	BL-2
4		Name various addressing modes and interpret each addressing mode with syntax and example.	14M	CO2	BL-2
5	a)	Write a program to move the contents of the memory location 0500H to register BX and to CX. Add immediate byte 05H to the data residing in memory location.	7M	C03	BL-3
		residing in memory location, whose address is computed using DS=2000H and offset=0600H. Store the result of addition in 0700H. Assume that the data is located in the segment specified by the data segment register DS which contain 2000H.			
	b)	Write an assembly language program to arrange a given series of hexadecimal bytes in ascending order.	7M	C03	BL-3
6		Assess the complete procedure for programming with an assembler with suitable example.	14M	C03	BL-5
7	a)	Illustrate the mechanism of Booth algorithm for multiplication.	7M	C04	BL-2
	b)	Analyze various possible modes of data transfer to and from peripherals.	7M	CO4	BL-4
8		How the instruction cycle in the CPU can be processed with a four-segment pipeline? Discuss in detail with an example.	14M	C05	BL-3