

## MARRI LAXMAN REDDY INSTITUTE OF TECHNOLOGY AND MANAGEMENT

(AN AUTONOMOUS INSTITUTION)
(Approved by AICTE, New Delhi & Affiliated to JNTUH, Hyderabad)
Accredited by NBA and NAAC with 'A' Grade & Recognized Under Section2(f) & 12(B)of the UGC act,1956

## II B.Tech II Sem Regular End Examination, July 2022 Computer Organization and Microprocessors (CSE, CSI, IT)

Time: 3 Hours. Max. Marks: 70

Note: 1. Question paper consists: Part-A and Part-B.

- 2. In Part A, answer all questions which carries 20 marks.
- 3. In Part B, answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions.

## PART-A

(10\*2 Marks = 20 Marks)

1. a)	Define computer architecture?	2M	CO1	BL1
b)	What is a program interrupt and interrupt service provider?	2M	CO1	BL1
c)	What do you mean by displacement in an instruction.	2M	CO2	BL1
d)	What is the use of assembler directives?	2M	CO2	BL1
e)	How a stack is operated?	2M	CO3	BL1
f)	How do you generate a delay in software?	2M	CO3	BL1
g)	What is the use of Booth's algorithm? What is its advantage?	2M	CO4	BL1
h)	How are peripheral devices different from central computer?	2M	CO4	BL1
i)	What is the difference between branch, jump and subroutine?	2M	CO5	BL1
j)	What is required to supervise the flow of information between auxiliary memory and main memory?	2M	C05	BL1

## PART-B

(10\*5 Marks = 50 Marks)

		(10 5 Ma	arks – 50 Marks)			
2	a)	With an example, explain the control timing signals?	5M	CO1	BL4	
	b)	With a neat diagram, explain the block diagram of a digital computer?	5M	CO1	BL4	
		OR				
3		Discuss different addressing modes in detail and with suitable examples.	10M	C01	BL2	
4	a) b)	Explain the physical memory organization in 8086 system.  What do you mean by pipelined architecture? How is it implemented in 8086 system?	5M 5M	CO2	BL4 BL1	
OR						
5		Explain 8086 architecture with a neat diagram.	10M	CO2	BL4	

6	a)	Write a program to add a data byte located at offset 0500H in 2000H segment to data byte available at 0600H in the same segment and store the result at 0700H in the same segment.	5M	CO3	BL3
	b)	Distinguish between assembly language and machine language?	5M	CO3	BL2
		OR	*		
7		What is a macro? How do you define a macro? Distinguish between subroutine and macro? What are the advantages and disadvantages of macros over subroutines?	10M	CO3	BL1
8	a)	How I/O devices are connected using I/O bus? What information do they exchange? Discuss with neat diagram.	5M	CO4	BL1
	b)	Why does DMA have priority over CPU, when both request a memory transfer? Explain.	5M	CO4	BL1
		OR			
9		Discuss about Booth's multiplier algorithm with flowchart using an example.	10M	CO4	BL6
			<b>51</b> 6	005	DIO
10	a)	Explain parallel processing with neat diagram.	5M	CO5	BL3
	b)	Discuss about array processors.	5M	CO5	BL6
		OR			
11		What is associative memory? Design the hardware organization of associative memory consisting of memory array and logic for m words with n bits per word?	10M	CO5	BL6

MLRS-R20

Course Code: 2040507 Roll No:

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