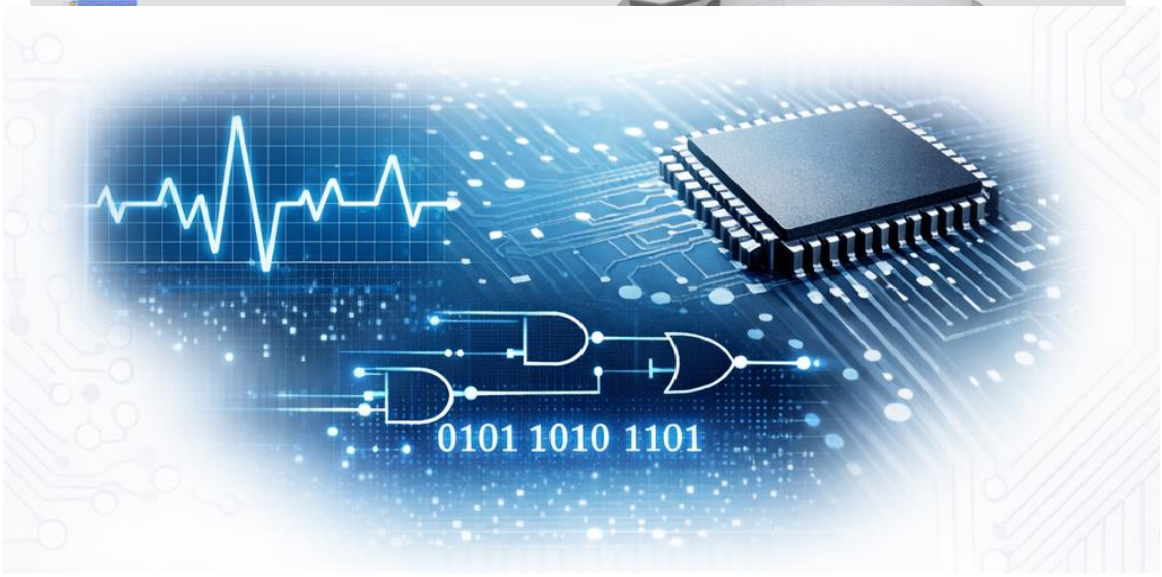
MARRI LAXMAN REDDY
INSTITUTE OF TECHNOLOGY AND MANAGEMENT
(AN AUTONOMOUS INSTITUTION)
(Approved by AICTE, New Delhi & Affiliated to JNTUH, Hyderabad)
Accredited by NBA and NAAC with 'A' Grade & Recognized Under Section2(f) & 12(B)of the UGC act,1956

Department of Electronics & Communication Engineering

ELECTRONIC DEVICES & DIGITAL ELECTRONICS LABORATORY MANUAL

II B.TECH -II SEMESTER (EEE)

R25 (MLRS) REGULATION



A.Y 2026-2027

CERTIFICATE

This is to certify that this manual is a bonafide record of practical work in the ***Electronic Devices & Digital Electronics Laboratory*** in **Fourth Semester of II-year B.Tech (EEE) Programme** during the academic year **2026-2027.** This book is prepared by **Mr. R. Kiran (Assistant Professor)** Department of Electronics and Communication Engineering.

LAB I/C **Head of the Department**

PREFACE

This laboratory lays a strong foundation for Electrical and Electronics Engineering students during the second year of their course. The Electronic Devices and Digital Electronics Laboratory is divided into two parts: Part-A and Part-B.

In Part-A, students design and analyze circuits related to Electronic Devices. In Part-B, students design and implement Digital Electronics circuits. Through these experiments, students gain practical knowledge and hands-on experience, which helps them develop the skills required to confidently handle electronic equipment used in the field of electronics.

By,

Mr. R. Kiran

ACKNOWLEDGEMENT

It was really a good experience, working with *Electronic Devices & Digital Electronics Laboratory*. First we would like to thank Dr. N. Srinivas, Associate Professor, HOD of Department of Electronics and Communication Engineering, Marri Laxman Reddy Institute of technology & Management for his concern and giving the technical support in preparing the document.

We are deeply indebted and gratefully acknowledge the constant support and valuable patronage of Dr. Ravi Prasad, Dean, Marri Laxman Reddy Institute of technology & Management for giving us this wonderful opportunity for preparing the *Electronic Devices & Digital Electronics Laboratory* manual.

We express our hearty thanks to Dr. R. Murali Prasad, Principal, Marri Laxman Reddy Institute of technology & Management, for timely corrections and scholarly guidance.

We express our hearty thanks to Dr. P. Sridhar, Director, Marri Laxman Reddy Institute of technology & Management, for timely corrections and scholarly guidance.

At last, but not the least I would like to thanks the entire ECE Department faculty those who had inspired and helped us to achieve our goal.

By,

Mr. R. Kiran

GENERAL INSTRUCTIONS

1. Students are instructed to come to Electronic Devices & Digital Electronics laboratory on time. Late comers are not entertained in the lab.
2. Students should be punctual to the lab. If not, the conducted experiments will not be repeated.
3. Students are expected to come prepared at home with the experiments which are going to be performed.
4. Students are instructed to display their identity cards before entering into the lab.
5. Students are instructed not to bring mobile phones to the lab.
6. Any damage/loss of equipments like transformers, transistors, CRO's etc., during the lab session, it is student's responsibility and penalty or fine will be collected from the student.
7. Students should update the records and lab observation books session wise. Before leaving the lab the student should get his lab observation book signed by the faculty.
8. Students should submit the lab records by the next lab to the concerned faculty members in the staffroom for their correction and return.
9. Students should not move around the lab during the lab session.
10. If any emergency arises, the student should take the permission from faculty member concerned in written format.
11. The faculty members may suspend any student from the lab session on disciplinary grounds.
12. Never copy the output from other students. Write down your own outputs.

SAFETY MEASURES

1. While working in the laboratory suitable precautions should be observed to prevent accidents.
2. Always follow the experimental instructions strictly.
3. Use the first aid box in case of any accident/mishap.
4. Never work in the laboratory unless a demonstrator or teaching assistant in present.
5. When the experiment is completed, students should disconnect the setup made by them, and should return all the components/instruments taken for the purpose.

INSTITUTION VISION AND MISSION

VISION

To be a globally recognized institution that fosters innovation, excellence, and leadership in education, research, and technology development, empowering students to create sustainable solutions for the advancement of society.

MISSION

To foster a transformative learning environment that empowers students to excel in engineering, innovation, and leadership.

To produce skilled, ethical, and socially responsible engineers who contribute to sustainable technological advancements and address global challenges.

To shape future leaders through cutting-edge research, industry collaboration, and community engagement.

Quality Policy

The management is committed in assuring quality service to all its stakeholders, students, parents, alumni, employees, employers, and the community.

Our commitment and dedication are built into our policy of continual quality improvement by establishing and implementing mechanisms and modalities ensuring accountability at all levels, transparency in procedures, and access to information and actions.

DEPARTMENT VISION, MISSION, PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES

Vision of the Department

To provide quality technical education in Electronics and Communication Engineering through research, innovation, striving for global recognition in specified domain, leadership, and sustainable societal solutions.

Mission of the Department

- **DM1:** To create a transformative learning environment that empowers students in electronics and communication engineering, fostering excellence in technical skills and leadership.
- **DM2:** To drive innovation through research, deliver a transformative education grounded in ethical principles, and nurture the development of professionals
- **DM3:** To cultivate strong industry partnerships, and engaging actively with the community for societal and technological progress.

Program Outcomes (POs)

Engineering Graduates will be able to:

1. **Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2. **Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
3. **Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4. **Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5. **Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an underst and ing of the limitations.
6. **The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. **Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8. **Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. **Individual and team work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. **Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11. **Project management and finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
12. **Life-long learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Program Specific Outcomes (PSOs)

1. Design, develop, fabricate and commission the electrical systems involving power generation, transmission, distribution and utilization.
2. Focus on the components of electrical drives with its converter topologies for energy conversion, management and auditing in specific applications of industry and sustainable rural development.
3. Gain the hands-on competency skills and other computing tools necessary for entry level position to meet the requirements of the employer.

Course Structure:

Level	Credits	Periods/Week	Prerequisites
UG	1	3	Entire Subject of Digital System Design & Electronics and Device Circuits

Evaluation Scheme:

Each laboratory will be evaluated for a total of 100 marks consisting of 40 marks for Continuous Internal Evaluation (CIE) and 60 marks for semester end lab examination. Out of 40 marks for internal evaluation:

- A write-up on day-to-day experiment(aim,components/procedure, expected outcome) which shall be evaluated for 10 marks
- 10 marks for viva-voce/ tutorial/ case study/ application/ poster presentation.
- Internal practical examination shall be evaluated for 10 marks.
- The remaining 10 marks are for Laboratory Project (Design/ Software / Hardware Model/ App Development/ Prototype).

Table 1: CIE marks distribution

Component				
Type of Assessment	Day to Day performance and viva voce examination	Final internal lab assessment	Laboratory Report / Project and Presentation	Total Marks
CIE marks	20	10	10	40

Continuous Internal Evaluation (CIE): Two CIE exams shall be conducted at the 8th week and 16th week of the semester; the average of the two CIEs will be taken into account. The CIE exam is conducted for 10 marks.

The Semester End Examination shall be conducted with an external examiner and the laboratory teacher. The external examiner shall be appointed from the other colleges which will be decided by the Head of the institution.

In the Semester End Examination held for 3 hours, total 60 marks are divided and allocated as shown below:

- 10 marks for write-up
- 15 for experiment/program
- 15 for evaluation of results
- 10 marks for presentation on another experiment/program in the same laboratory course and
- 10 marks for viva-voce on concerned laboratory course.

Course Objectives:

The students will try to learn

- The characteristics and applications of semiconductor devices such as diodes and transistors.
- Designing and analyzing basic rectifiers, regulators, amplifiers, and switching circuits
- Implementation and verification of digital logic functions using basic and universal logic gates
- Designing of combinational and sequential digital circuits
- Practical skills in circuit construction, testing, troubleshooting, and simulation of electronic systems.

Course Outcomes:

After successful completion of the course, students shall be able to

- Analyze and interpret the characteristics of electronic devices like diodes and BJTs
- Capable of designing and evaluating rectifier, regulator, and amplifier circuits
- Demonstrate the ability to implement and simplify logic functions using various logic gates
- Design, construct, digital circuits such as adders, converters, and shift registers
- Gain hands-on proficiency in using simulation software and electronic instruments for circuit analysis and verification

Course Outcomes (CO's) – Program Outcomes (PO's) Mapping:

CO1: Analyze and interpret the characteristics of electronic devices like diodes and BJTs.
CO2: Capable of designing and evaluating rectifier, regulator, and amplifier circuits.
CO3: Demonstrate the ability to implement and simplify logic functions using various logic gates.
CO4: Design, construct, digital circuits such as adders, converters, and shift registers.
CO5: Gain hands-on proficiency in using simulation software and electronic instruments for circuit analysis and verification.

MAPPING OF EACH CO WITH PO(s),PSO(s):

Course Outcomes	PROGRAM OUTCOMES														
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO1	✓	✓	✓	✓	✓	✓	-	-	-	-	-	✓	✓		✓
CO2	✓	✓	✓	✓	✓	✓	-	-	-	-	-	✓	-	-	✓
CO3	✓	✓	✓	✓	✓	✓	-	-	-	-	-	✓	-	-	✓
CO4	✓	✓	✓	✓	✓	✓	-	-	-	-	-	✓	✓	✓	✓
CO5	✓	✓	✓	✓	✓	-	-	-	-	-	-	✓	✓	✓	✓

JUSTIFICATIONS FOR CO – PO / PSO MAPPING - DIRECT:

Course Outcomes	PO'S/ PSO'S	Justification for mapping (Students will be able to)	No. of Key Competencies
CO1	PO1	1. Scientific principles and methodology 2. Mathematical principles 3. Own and / or other engineering disciplines to integrate / support study of their own engineering discipline.	3
	PO2	1. Problem or opportunity identification 2. Problem statement and system definition 3. Problem formulation and abstraction 4. Information and data collection 5. Model translation 6. Validation 7. Experimental design 8. Solution development or experimentation /Implementation 9. Interpretation of results	9
	PO3	1. Investigate and define a problem and identify constraints including environmental and sustainability limitations, health and safety and risk assessment issues; 2. Understand customer and user needs and the	6

		importance of considerations such as aesthetics; 3. Use creativity to establish innovative solutions; 4. Manage the design process and evaluate outcomes. 5. Knowledge of management techniques which may be used to achieve engineering objectives within that context; 6. Understanding of the requirement for engineering activities to promote sustainable development;	
	PO4	1. Knowledge of characteristics of particular materials, equipment, processes, or products; 2. Workshop and laboratory skills; 3. Understanding of contexts in which engineering knowledge can be applied (example, operations and management, technology development, etc.); 4. Understanding use of technical literature and other information sources Awareness of nature of intellectual property and contractual issues; 5. Understanding of appropriate codes of practice and industry standards; 6. Ability to work with technical uncertainty. 7. Understanding of engineering principles and the ability to apply them to analyze key engineering processes; 8. Ability to apply quantitative methods and computer software relevant to their engineering discipline, in order to solve engineering problems; 9. Understanding of and ability to apply a systems approach to engineering problems.	9
	PO5	1. Computer software/ simulation packages/ diagnostic equipment/ technical library resources/ literature search tools.	`1
	PO6	1. Knowledge of management techniques which may be used to achieve engineering objectives within that context; 2. Understanding of the requirement for engineering activities to promote sustainable development;	2

	PO12	1. Keeping current in ECE and advanced engineering concepts 2. Personal continuing education efforts 3. Ongoing learning – stays up with industry trends/ new technology 4. Continued personal development	4
	PSO1	1. Adopt the engineering professional code and conduct 2. Sustainable and Compliant Design	2
	PSO3	1. Adopt technical library resources and literature search. 2. Research, analysis, problem solving	2
CO2	PO1	1. Scientific principles and methodology 2. Mathematical principles 3. Own and / or other engineering disciplines to integrate / support study of their own engineering discipline.	3
	PO2	1. Problem or opportunity identification 2. Problem statement and system definition 3. Problem formulation and abstraction 4. Information and data collection 5. Model translation 6. Validation 7. Experimental design 8. Solution development or experimentation /Implementation 9. Interpretation of results	9
	PO3	1. Investigate and define a problem and identify constraints including environmental and sustainability limitations, health and safety and risk assessment issues; 2. Understand customer and user needs and the importance of considerations such as aesthetics; 3. Use creativity to establish innovative solutions; 4. Manage the design process and evaluate outcomes. 5. Knowledge of management techniques which may be used to achieve engineering objectives within that context; 6. Understanding of the requirement for	6

		engineering activities to promote sustainable development;	
	PO4	1. Knowledge of characteristics of particular materials, equipment, processes, or products; 2. Workshop and laboratory skills; 3. Understanding of contexts in which engineering knowledge can be applied (example, operations and management, technology development, etc.); 4. Understanding use of technical literature and other information sources Awareness of nature of intellectual property and contractual issues; 5. Understanding of appropriate codes of practice and industry standards; 6. Ability to work with technical uncertainty. 7. Understanding of engineering principles and the ability to apply them to analyze key engineering processes; 8. Ability to apply quantitative methods and computer software relevant to their engineering discipline, in order to solve engineering problems; 9. Understanding of and ability to apply a systems approach to engineering problems.	9
	PO5	1. Computer software/simulation packages/diagnostic equipment/technical library resources/ literature search tools.	1
	PO6	1. Knowledge of management techniques which may be used to achieve engineering objectives within that context; 2. Understanding of the requirement for engineering activities to promote sustainable development;	2
	PO12	1. Keeping current in ECE and advanced engineering concepts 2. Personal continuing education efforts 3. Ongoing learning – stays up with industry trends/ new technology 4. Continued personal development	4
	PSO3	1. Adopt technical library resources and literature search. 2. Research, analysis, problem solving	2

CO3	PO1	1. Scientific principles and methodology 2. Mathematical principles 3. Own and / or other engineering disciplines to integrate / support study of their own engineering discipline.	3
	PO2	1. Problem or opportunity identification 2. Problem statement and system definition 3. Problem formulation and abstraction 4. Information and data collection 5. Model translation 6. Validation 7. Experimental design 8. Solution development or experimentation /Implementation 9. Interpretation of results	9
	PO3	1. Investigate and define a problem and identify constraints including environmental and sustainability limitations, health and safety and risk assessment issues; 2. Understand customer and user needs and the importance of considerations such as aesthetics; 3. Use creativity to establish innovative solutions; 4. Manage the design process and evaluate outcomes. 5. Knowledge of management techniques which may be used to achieve engineering objectives within that context; 6. Understanding of the requirement for engineering activities to promote sustainable development;	6
	PO4	1. Knowledge of characteristics of particular materials, equipment, processes, or products; 2. Workshop and laboratory skills; 3. Understanding of contexts in which engineering knowledge can be applied (example, operations and management, technology development, etc.); 4. Understanding use of technical literature and other information sources Awareness of nature of intellectual property and contractual issues; 5. Understanding of appropriate codes of practice and industry standards; 6. Ability to work with technical uncertainty.	9

		7. Understanding of engineering principles and the ability to apply them to analyze key engineering processes; 8. Ability to apply quantitative methods and computer software relevant to their engineering discipline, in order to solve engineering problems; 9. Understanding of and ability to apply a systems approach to engineering problems.	
	PO5	1. Computer software/ simulation packages/ diagnostic equipment/ technical library resources/ literature search tools.	1
	PO6	1. Knowledge of management techniques which may be used to achieve engineering objectives within that context; 2. Understanding of the requirement for engineering activities to promote sustainable development;	2
	PO12	1. Keeping current in ECE and advanced engineering concepts 2. Personal continuing education efforts 3. Ongoing learning – stays up with industry trends/ new technology 4. Continued personal development	4
	PSO3	1. Adopt technical library resources and literature search. 2. Research, analysis, problem solving	2
CO4	PO1	1. Scientific principles and methodology 2. Mathematical principles 3. Own and / or other engineering disciplines to integrate / support study of their own engineering discipline.	3
	PO2	1. Problem or opportunity identification 2. Problem statement and system definition 3. Problem formulation and abstraction 4. Information and data collection 5. Model translation 6. Validation 7. Experimental design 8. Solution development or experimentation /Implementation 9. Interpretation of results	9
	PO3	1. Investigate and define a problem and identify	6

		constraints including environmental and sustainability limitations, health and safety and risk assessment issues; 2. Understand customer and user needs and the importance of considerations such as aesthetics; 3. Use creativity to establish innovative solutions; 4. Manage the design process and evaluate outcomes. 5. Knowledge of management techniques which may be used to achieve engineering objectives within that context; 6. Understanding of the requirement for engineering activities to promote sustainable development;	
	PO4	1. Knowledge of characteristics of particular materials, equipment, processes, or products; 2. Workshop and laboratory skills; 3. Understanding of contexts in which engineering knowledge can be applied (example, operations and management, technology development, etc.); 4. Understanding use of technical literature and other information sources Awareness of nature of intellectual property and contractual issues; 5. Understanding of appropriate codes of practice and industry standards; 6. Ability to work with technical uncertainty. 7. Understanding of engineering principles and the ability to apply them to analyze key engineering processes; 8. Ability to apply quantitative methods and computer software relevant to their engineering discipline, in order to solve engineering problems; 9. Understanding of and ability to apply a systems approach to engineering problems.	9
	PO5	1. Computer software/ simulation packages/ diagnostic equipment/ technical library resources/ literature search tools.	1
	PO6	1. Knowledge of management techniques which may be used to achieve engineering objectives within that context;	2

		2. Understanding of the requirement for engineering activities to promote sustainable development;	
	PO12	1. Keeping current in ECE and advanced engineering concepts 2. Personal continuing education efforts 3. Ongoing learning – stays up with industry trends/ new technology 4. Continued personal development	4
	PSO1	1. Adopt the engineering professional code and conduct	1
	PSO2	1. Adopt the engineering professional code and conduct.	1
	PSO3	1. Adopt technical library resources and literature search. 2. Research, analysis, problem solving	2
CO5	PO1	1. Scientific principles and methodology 2. Mathematical principles 3. Own and / or other engineering disciplines to integrate / support study of their own engineering discipline.	3
	PO2	1. Problem or opportunity identification 2. Problem statement and system definition 3. Problem formulation and abstraction 4. Information and data collection 5. Model translation 6. Validation 7. Experimental design 8. Solution development or experimentation /Implementation 9. Interpretation of results	9
	PO3	1. Investigate and define a problem and identify constraints including environmental and sustainability limitations, health and safety and risk assessment issues; 2. Understand customer and user needs and the importance of considerations such as aesthetics; 3. Use creativity to establish innovative solutions; 4. Manage the design process and evaluate outcomes. 5. Knowledge of management techniques which may be used to achieve engineering objectives	6

		within that context; 6. Understanding of the requirement for engineering activities to promote sustainable development;	
	PO4	1. Knowledge of characteristics of particular materials, equipment, processes, or products; 2. Workshop and laboratory skills; 3. Understanding of contexts in which engineering knowledge can be applied (example, operations and management, technology development, etc.); 4. Understanding use of technical literature and other information sources Awareness of nature of intellectual property and contractual issues; 5. Understanding of appropriate codes of practice and industry standards; 6. Ability to work with technical uncertainty. 7. Understanding of engineering principles and the ability to apply them to analyze key engineering processes; 8. Ability to apply quantitative methods and computer software relevant to their engineering discipline, in order to solve engineering problems; 9. Understanding of and ability to apply a systems approach to engineering problems.	9
	PO5	1. Computer software/ simulation packages/ diagnostic equipment/ technical library resources/ literature search tools.	1
	PO6	1. Knowledge of management techniques which may be used to achieve engineering objectives within that context; 2. Understanding of the requirement for engineering activities to promote sustainable development;	2
	PO12	1. Keeping current in ECE and advanced engineering concepts 2. Personal continuing education efforts 3. Ongoing learning – stays up with industry trends/ new technology	4

		4. Continued personal development	
	PSO1	1. Adopt the engineering professional code and conduct	1
	PSO2	1. Adopt the engineering professional code and conduct.	1
	PSO3	1. Adopt technical library resources and literature search. 2. Research, analysis, problem solving	2

TOTAL COUNT OF KEY COMPETENCIES FOR CO – (PO, PSO) MAPPING:

Course Outcomes	PROGRAM OUTCOMES														
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
	4	10	10	10	4	5	4	4	10	5	10	8	6	10	8
CO1	3	9	6	9	1	2	-	-	-	-	-	4	2	-	2
CO2	3	9	6	9	1	2	-	-	-	-	-	4	-	-	2
CO3	3	9	6	9	1	2	-	-	-	-	-	4	-	-	2
CO4	3	9	6	9	1	2	-	-	-	-	-	4	1	1	2
CO5	3	9	6	9	1	2	-	-	-	-	-	4	1	1	2

PERCENTAGE OF KEY COMPETENCIES FOR CO – (PO/ PSO):

Course Outcomes	PROGRAM OUTCOMES														
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO1	75	90	60	90	25	40	-	-	-	-	-	50	33	-	25
CO2	75	90	60	90	25	40	-	-	-	-	-	50	-	-	25
CO3	75	90	60	90	25	40	-	-	-	-	-	50	-	-	25
CO4	75	90	60	90	25	40	-	-	-	-	-	50	17	10	25
CO5	75	90	60	90	25	40	-	-	-	-	-	50	17	10	25

COURSE ARTICULATION MATRIX (PO – PSO MAPPING):

CO'S and PO'S, CO'S and PSO'S on the scale of 0 to 3, 0 being no correlation, 1 being the low correlation, 2 being medium correlation and 3 being high correlation.

0 - 0≤ C≤ 5% – No correlation,
1-5 <C≤ 40% – Low/ Slight
2 - 40 % <C < 60% –Moderate
3 - 60% ≤ C < 100% – Substantial /High

Course Outcomes	PROGRAM OUTCOMES														
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO1	3	3	3	3	1	2	-	-	-	-	-	2	1	-	1
CO2	3	3	3	3	1	2	-	-	-	-	-	2	-	-	1
CO3	3	3	3	3	1	2	-	-	-	-	-	2	-	-	1
CO4	3	3	3	3	1	2	-	-	-	-	-	2	1	1	1
CO5	3	3	3	3	1	2	-	-	-	-	-	2	1	1	1
Total	15	15	15	15	5	10	-	-	-	-	-	10	3	2	5
Average	3	3	3	3	1	2	-	-	-	-	-	2	1	1	1

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ACADEMIC CALENDAR 2025 - 26

2025 - B.Tech. I & II Semesters (MLRS-BT25)

I Semester

SNo.	Description	Period		Duration
		From	To	
1	Induction Program	11.08.2025	16.08.2025	1 Week
2	Commencement of Class work	**18.08.2025**		
3	1st Spell of instructions	18.08.2025	27.09.2025	6 Weeks
4	**Dussehra Recess**	29.09.2025	04.10.2025	1 Week
5	1st Spell of instructions (Contd.)	06.10.2025	18.10.2025	2 Weeks
6	First Mid Term Examinations	20.10.2025	25.10.2025	1 Week
7	Parent-Teacher Meeting	**01.11.2025**		
8	2nd Spell of instructions	27.10.2025	13.12.2025	7 Weeks
9	Second Mid Term Examinations	15.12.2025	20.12.2025	1 Week
10	Semester End Examinations/Supply	22.12.2025	03.01.2026	2 Weeks
11	Practical End Examinations	05.01.2026	10.01.2026	1 Week
12	**Sankranthi Recess**	12.01.2026	17.01.2026	1 Week

II Semester

SNo.	Description	Period		Duration
		From	To	
1	Commencement of Class work	**19.01.2026**		
2	1st Spell of instructions	19.01.2026	14.03.2026	8 Weeks
3	First Mid Term Examinations	16.03.2026	21.03.2026	1 Week
4	2nd Spell of instructions	23.03.2026	09.05.2026	7 Weeks
5	Last date of instructions	**09.05.2026**		
6	**Summer Vacation/Internship**	11.05.2026	06.06.2026	4 Weeks
7	Second Mid Term Examinations	08.06.2026	13.06.2026	1 Week
8	Semester End Examinations/Supply	15.06.2026	27.06.2026	2 Weeks
9	Practical End Examinations	29.06.2026	04.07.2026	1 Week

***Commencement of III Semester class work: 06.07.2026**

Dr.B.Ravi Prasad Dean Academics
Bhushan Kundeti Controller of Examinations
Dr.R.Murali Prasad Principal
Dr.P.Sridhar Director

LAB TIME TABLE

ROOM NO: SR-110

NAME OF THE LAB: ED & DE LAB **A.Y:** 2026-2027

BRANCH: EEE **W.E.F:**

SEMESTER: II

PERIOD	1st	2nd	3rd	12:25 - 01:15	4th	5th	6th
TIME	09:40 - 10:35	10:35 - 11:30	11:30 - 12:25		01:15 - 02:10	02:10 - 03:05	03:05 - 04:00
DAY							
MON				LUNCH	ED & DE LAB 2EEE		
TUE							
WED							
THU							
FRI							
SAT							

Time Table I/C **Time Tables C/D** **HOD – ECE**

B.Tech II Year Syllabus (MLRS-R25) **MLRITM-EEE**

MARRI LAXMAN REDDY INSTITUTE OF TECHNOLOGY AND MANAGEMENT (AUTONOMOUS)

2540482: ELECTRONIC DEVICES & DIGITAL ELECTRONICS LABORATORY

II Year B.Tech EEE II –Sem

L	T	P	C
0	0	2	1

Course Overview:

This course offers hands-on experience in both analog and digital electronics through hardware and simulation-based experiments. Students will study the characteristics and applications of diodes, transistors, and amplifiers, along with the design of fundamental digital circuits. Emphasis is placed on circuit analysis, implementation, and verification using both practical and software tools.

Pre-requisite:

Electronic Device Circuits

Course Objectives:

The students will try to learn

- The characteristics and applications of semiconductor devices such as diodes and transistors.
- Designing and analyzing basic rectifiers, regulators, amplifiers, and switching circuits
- Implementation and verification of digital logic functions using basic and universal logic gates
- Designing of combinational and sequential digital circuits
- Practical skills in circuit construction, testing, troubleshooting, and simulation of electronic systems.

Course Outcomes:

After successful completion of the course, students shall be able to

- Analyze and interpret the characteristics of electronic devices like diodes and BJTs
- Capable of designing and evaluating rectifier, regulator, and amplifier circuits
- Demonstrate the ability to implement and simplify logic functions using various logic gates
- Design, construct, digital circuits such as adders, converters, and shift registers
- Gain hands-on proficiency in using simulation software and electronic instruments for circuit analysis and verification

PART-A: Electronic Devices and Circuits experiments

Hardware-Based Experiments:

1. Study the I–V characteristics of a PN junction diode in forward and reverse bias to determine cut-in voltage and dynamic resistance.
2. Examine the reverse bias characteristics of a Zener diode and demonstrate its application as a voltage regulator under varying conditions.
3. Design and analyse half-wave and full-wave rectifiers (centre-tap) with and without capacitor filters to evaluate ripple factor and output voltage.
4. Implement clipper and clamper circuits to observe waveform shaping through positive, negative, and biased configurations.
5. Plot the input and output characteristics of a BJT in common emitter configuration to determine input/output resistance current gain.
6. Construct and analyse a Common Base (CB) configuration of a BJT to study input-output characteristics and determine current gain (α) and input/output resistance.

Software-Based Simulation Experiments

7. Simulate a Zener diode-based voltage regulator to study voltage stabilization against varying supply voltages.
8. Simulate a common emitter amplifier with and without emitter bypass capacitor to analyse the effect on voltage gain and signal amplification.

Hardware Requirements:

1. Regulated DC Power Supply (0–30V)
2. Function Generator
3. Digital Multimeter
4. Cathode Ray Oscilloscope (CRO) or DSO
5. Breadboards and Connecting Wires
6. Resistors, Capacitors, Diodes (1N4007, Zener Diodes)
7. BJTs (e.g., BC107, 2N2222), JFETs (e.g., J201), MOSFETs (e.g., IRF540N)
8. Trainer Kits (optional but preferred for ease)

Software Requirements (Any one of the listed tools or equivalent):

1. LTSpice (Free from Analog Devices)
2. NI Multisim (Academic License or Student Version)
3. Proteus Design Suite (Simulation and PCB Design)
4. TINA-TI (Free from Texas Instruments)
5. PSPICE for TI or OrCAD Lite
6. Windows PC or Laptop with minimum 4GB RAM and i3 processor or better

PART-B. Digital Electronics Experiments

1. Realization of Boolean Expressions using Gates
2. Design and realization logic gates using universal gates
3. Generation of clock using NAND/NOR gates
4. Design a 4 – bit Adder / Subtractor
5. Design and realization a 4 – bit gray to Binary and Binary to Gray Converter
6. Design and realization of an 8-bit parallel load and serial out shift register using flip-flops.
7. Design and realization 8x1 using 2x1 mux
8. Design and realization 4-bit comparator.

NOTE: Minimum of 6 experiments to be conducted from each PART.

ELECTRONIC DEVICES & DIGITAL ELECTRONICS LABORATORY

Virtual lab details

Name of the Virtual Lab: ED&DE with Virtual Laboratory

Virtual Lab Host Institute: IIT Delhi, India

URL/Link to Lab: https://www.vlab.co.in/

Academic Year: 2026-2027

Semester: II

List of Experiments Available in Virtual Lab

1. VI Characteristics of a Diode
2. Zener Diode Voltage Regulator
3. Full Wave Rectification
4. BJT Common Emitter Characteristics
5. Analysis and Synthesis of Boolean Expressions using Basic Logic Gates
6. Generation of clock using NAND/NOR gates
7. Analysis and Synthesis of Arithmetic Expressions using Adders/Subtractors
8. Analysis and Binary to Gray Code and Gray to Binary Code Converter
9. Analysis and Synthesis of Multi-bit Sequential Circuits using Shift Registers
10. Analysis and Synthesis of Logic Functions using Multiplexers
11. Analysis and Synthesis of Boolean Relations using Digital Comparators

ELECTRONIC DEVICES & DIGITAL ELECTRONICS LABORATORY

LAB PLANNER

S.No	Experiment	CO	Virtual Lab Availability	Date planned	Date conducted
1	PN Junction Diode Characteristics: Forward and Reverse Bias.	1	Yes		
2	Reverse Bias Characteristics of a Zener Diode	1	Yes		
3	Half-Wave and Full-Wave Rectifiers With and Without Capacitor Filters	2	Yes		
4	Clipper and Clamper Circuits	1	No		
5	Common Emitter amplifier characteristics.	1	Yes		
6	Common Base (CB) Configuration of a BJT	1	No		
	MID-I				
7	Simulate a Zener diode-based voltage regulator	5	Yes		
8	Simulate a common emitter amplifier with and without emitter bypass capacitor	5	Yes		
9	Realization of Boolean Expressions using Gates	4	Yes		
10	Design and realization logic gates using universal gates	4	Yes		
11	Generation of clock using NAND/NOR gates	4	Yes		
12	Design a 4-bit Adder / Subtractor	4	Yes		
13	Design and realization a 4 – bit gray to Binary and Binary to Gray Converter	4	Yes		
14	Design and realization of an 8-bit parallel load and serial out shift register using flip-flops	5	Yes		
15	Design and realization 8x1 MUX using 2x1 MUX	4	Yes		
16	Design and realization 4-bit comparator	4	Yes		
	MID-II				

ELECTRONIC DEVICES & DIGITAL ELECTRONICS LABORATORY

LAB PLANNER

Date planed																		
Date conducted																		
Roll Number	**Exp No**	**CO**	**VL**	**Exp No**	**CO**	**VL**	**Exp No**	**CO**	**VL**	**Exp No**	**CO**	**VL**	**Exp No**	**CO**	**VL**	**Exp No**	**CO**	**VL**	
247Y1A0201	1	1	Y	2	1	Y	3	2	Y	4	1	N	5	1	Y	6	1	N	
247Y1A0202	1	1	Y	2	1	Y	3	2	Y	4	1	N	5	1	Y	6	1	N	**M**
247Y1A0203	1	1	Y	2	1	Y	3	2	Y	4	1	N	5	1	Y	6	1	N	**I**
247Y1A0204	1	1	Y	2	1	Y	3	2	Y	4	1	N	5	1	Y	6	1	N	**D**
247Y1A0205	1	1	Y	2	1	Y	3	2	Y	4	1	N	5	1	Y	6	1	N	-
247Y1A0206	1	1	Y	2	1	Y	3	2	Y	4	1	N	5	1	Y	6	1	N	**I**

Note: VL*-Virtual Lab Availability

Date planed																		
Date conducted																		
Roll Number	**Exp No**	**CO**	**VL**	**Exp No**	**CO**	**VL**	**Exp No**	**CO**	**VL**	**Exp No**	**CO**	**VL**	**Exp No**	**CO**	**VL**	**Exp No**	**CO**	**VL**	
247Y1A0201	7	4	Y	8	4	Y	9	4	Y	10	4	Y	11	4	Y	12	5	Y	
247Y1A0202	7	4	Y	8	4	Y	9	4	Y	10	4	Y	11	4	Y	12	5	Y	**M**
247Y1A0203	7	4	Y	8	4	Y	9	4	Y	10	4	Y	11	4	Y	12	5	Y	**I**
247Y1A0204	7	4	Y	8	4	Y	9	4	Y	10	4	Y	11	4	Y	12	5	Y	**D**
247Y1A0205	7	4	Y	8	4	Y	9	4	Y	10	4	Y	11	4	Y	12	5	Y	**-**
247Y1A0206	7	4	Y	8	4	Y	9	4	Y	10	4	Y	11	4	Y	12	5	Y	**II**

Note: VL*-Virtual Lab Availability

ELECTRONIC DEVICES & DIGITAL ELECTRONICS LABORATORY

RUBRICS USED TO ASSESS LEARNINGS IN LABORATORIES

1. RUBRICS FOR DAY TO DAY EVALUATION

Parameter	Max Marks	Level-1 (Very Poor)	Level-2 (Poor)	Level-3 (Average)	Level-4 (Good)	Level-5 (Excellent)
Observation Book	05	No observations or irrelevant data. (0–1)	Incomplete or incorrect data. (2)	Basic values with some errors. (3)	Mostly correct with good format. (4)	Fully correct, clear, and well-formatted. (5)
Record Writing	05	Not submitted. (0-1)	Submitted but mostly incomplete. (2)	Submitted with some missing/wrong parts. (3)	Submitted with minor issues. (4)	Fully complete, correct algorithm & flowchart. (5)
Result	05	No result or major errors. (0–1)	Result partially obtained. (2)	Acceptable result with limited error. (3)	Near-correct result and reasonable error. (4)	Accurate result. (5)
Viva-Voce	05	Did not answer any questions. (1)	Answered very few questions. (2)	Answered some questions with help. (3)	Answered most questions correctly. (4)	Answered all questions accurately. (5)

ELECTRONIC DEVICES & DIGITAL ELECTRONICS LABORATORY

2. RUBRICS FOR INTERNAL EVALUATION

Criterion	Max Marks	Level-1 *(Very Poor)*	Level-2 *(Poor)*	Level-3 *(Average)*	Level-4 *(Good)*	Level-5 *(Excellent)*
Design/Tool/Apparatus Selection	2 Marks	Incorrect tool/design and no reasoning. **(0)**	Tool/design selection attempted with unclear logic. **(0.5)**	Satisfactory selection with partial justification. **(1)**	Correct selection and proper analysis with few errors. **(1.5)**	Smart selection with accurate, relevant analysis. **(2)**
Execution (Code/Debug/Run) /Analysis/Method Used	4 Marks	Did not attempt or completely failed to execute. **(0)**	Attempted but unable to proceed or with major errors. **(1)**	Partial execution with some logic/syntax errors. **(2)**	Mostly correct execution with minimal help. **(3)**	Fully correct and independently executed program. **(4)**
Results& Documentation	2 Marks	Incomplete or poorly presented. **(0)**	Basic structure but lacks clarity or formatting. **(0.5)**	Complete but generic or with formatting issues. **(1)**	Well-structured and mostly clear. **(1.5)**	Well-organized, professional, and engaging documentation. **(2)**
Viva-Voce (Understanding of Concepts)	2 Marks	No understanding; could not answer questions. **(0)**	Answered a few with difficulty. **(0.5)**	Answered half the questions with basic clarity. **(1)**	Good understanding with confident answers. **(1.5)**	Answered all questions with clarity and depth. **(2)**

ELECTRONIC DEVICES & DIGITAL ELECTRONICS LABORATORY

3. RUBRICS FOR SEMESTER END EXAMINATIONS

Criterion	Max Marks	Level-1 (Very Poor (*0–2 marks)*	Level-2 (Poor)*(3–4 marks)*	Level-3 (Average)*(5–6 marks)*	Level-4 (Good)*(7–9 marks)*	Level-5 (Excellent)*(10–12 marks)*
Preparedness for the Experiment	12 marks	No clarity on objective or procedure. Unable to explain basics.	Limited idea of the objective/procedure. Needed prompting.	Has basic understanding; minor gaps in concept or preparation.	Well-prepared, with clear understanding of steps and background.	Fully prepared with strong conceptual clarity and confident explanation.
Performance in the Laboratory	12 marks	Unable to perform experiment. Relied entirely on examiner's help.	Performed with multiple errors and constant support.	Performed with some errors; required occasional help.	Performed mostly independently with minimal support.	Performed independently, efficiently, and with precision.
Calculations & Graphs	12 marks	No or incorrect calculations. Graphs missing or irrelevant.	Multiple calculation errors. Graphs/plots inaccurate or poorly labelled.	Calculations partially correct. Graphs present but with some flaws.	Correct calculations and graphs with minor errors.	Accurate calculations and well-labelled graphs with proper interpretation.
Results & Error Analysis	12 marks	No result or invalid result. No error analysis attempted.	Incorrect result with vague or no error discussion.	Acceptable result. Error analysis attempted but limited.	Correct result with sound error discussion.	Accurate result with detailed and relevant error analysis.
Viva-Voce (Subject Knowledge)	12 marks	Unable to answer any questions. No conceptual understanding.	Answered few questions with poor logic.	Answered half of the questions with average understanding.	Answered most questions with clarity and confidence.	Answered all questions with depth, clarity, and reasoning.

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PART-A

Experiment No. 1

Study the I–V characteristics of a PN junction diode in forward and reverse bias to determine cut-in voltage and dynamic resistance..

AIM:

To plot the V-I characteristics of a PN junction diode in both forward and reverse directions.

APPARATUS:

S.No	Device	Range / Rating	Quantity
1	Semiconductor diode trainer Board Containing DC Power Supply. Diode (Silicon) Diode (Germanium) Carbon Film Resistor	 (0-15) V 1N 4007 OA79 1 KΩ, 1/2 W	 1 1 1 1
2	DC Voltmeter DC Voltmeter	(0-1) V (0-20) V	1 1
3	DC Ammeter DC Ammeter	(0-200) μA (0-20) mA	1 1
4	Connecting wires	As required	

THEORY:

A p-n junction diode conducts only in one direction. The V-I characteristics of the diode are curve between voltage across the diode and current through the diode. When external voltage is zero, circuit is open and the potential barrier does not allow the current to flow. Therefore, the circuit current is zero. When P-type (Anode is connected to +ve terminal and n- type (cathode) is connected to –ve terminal of the supply voltage, is known as forward bias. The potential barrier is reduced when diode is in the forward biased condition. At some forward voltage, the potential barrier altogether eliminated and current starts flowing through the diode and also in the circuit. The diode is said to be in ON state. The current increases with increasing forward voltage. When N-type (cathode)

is connected to +ve terminal and P-type (Anode) is connected –ve terminal of the supply voltage is known as reverse bias and the potential barrier across the junction increases. Therefore, the junction resistance becomes very high and a very small current (reverse saturation current) flows in the circuit. The diode is said to be in OFF state. The reverse bias current due to minority charge carriers.

CIRCUIT DIAGRAM :

Forward bias:

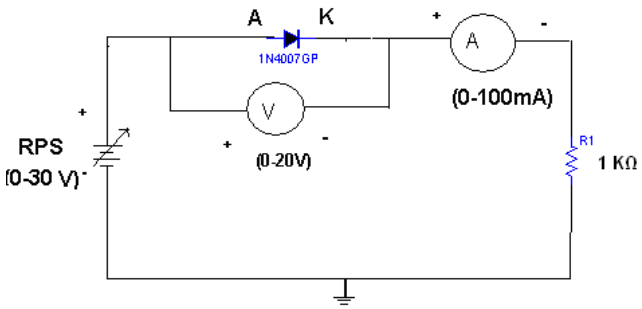


Figure 1.1 Circuit diagram of Forward bias of a PN junction Diode

Reverse bias:

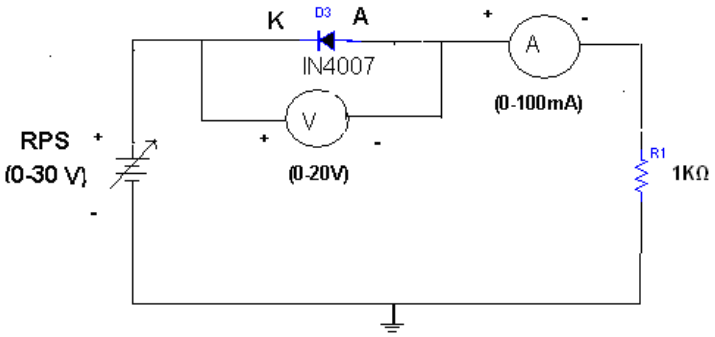


Figure 1.2 Circuit diagram of Forward bias of a PN junction Diode

PROCEDURE:

Forward Bias:

1. Connect the circuit as shown in figures (1)
2. Vary the supply voltage E_S in steps and note down the corresponding values of E_f and I_f as shown in the tabular column.

Reverse Bias:

1. Connect the circuit as shown in figure (2).
2. Repeat the procedure as in forward bias and note down the corresponding Values of E_r and I_r as shown in the tabular column.

TABULAR COLUMN:

FORWARD BIAS

V_S(Volts)	Vf (Volts)	If (mA)

REVERSE BIAS

VS()	Vr(Volts)	Ir(mA)

EXPECTED GRAPH:

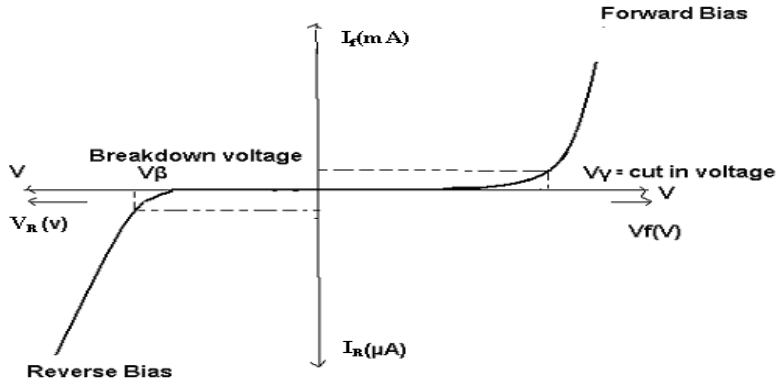


Figure 1.3 Expected waveform of a PN junction Diode characteristics

PRECAUTIONS:

1. Check the wires for continuity before use.
2. Keep the power supply at Zero volts before Start.
3. All the contacts must be intact.

RESULT:

Thus, V-I characteristics of a PN junction diode in both forward and reverse bias are studied and plotted

REAL TIME APPLICATIONS:

1. Rectification (AC to DC Conversion)

Used in half-wave, full-wave, and bridge rectifiers

Found in mobile chargers, power adapters, TVs, computers

2. Electronic Switching

Acts as an ON/OFF switch in digital and logic circuits

Used in signal routing and control circuits

3. Signal Detection (Demodulation)

Used in AM radio receivers

Extracts audio signal from modulated carrier wave

4.Clipping Circuits

Used to remove unwanted voltage levels

Applied in wave shaping and signal protection

5. Clamping Circuits

Used to shift voltage level of a signal

Applied in TV receivers and communication systems

6. Protection Circuits

Protects circuits from reverse polarity

Used in power supply inputs

7. Voltage Multipliers

Used in voltage doubler, tripler circuits

Applications in CRT displays, X-ray machines

8. Logic Gates

Used in diode logic (AND, OR gates)

Simple digital circuits

9. Solar Panels (Bypass Diodes)

Prevents reverse current flow

Improves efficiency and safety

VIVA QUESTIONS:

1. What is P-N junction diode?
2. What is doping why doping is necessary?
3. Difference between P-type and N-type semiconductor materials?
4. What is diode equation?
5. What is an ideal diode?
6. Define depletion region of a diode?
7. What is meant by transition & space charge capacitance of a diode?
8. Is the V-I relationship of a diode Linear or Exponential?
9. Define cut-in voltage of a diode and specify the values for Si and Ge diodes?
10. What are the applications of a p-n diode?
11. Draw the ideal characteristics of P-N junction diode?
12. What is the diode equation?
13. What is the break down voltage?
14. What is the effect of temperature on PN junction diodes?
15. What is PIV?
16. What is Forward bias?
17. What is Reverse bias?
18. What is Forward voltage?
19. What is Reverse current?
20. What is an ideal diode?
21. What is Break down voltage?
22. What is cut-in volatge?
23. Is the V-I relationship of a diode Linear or Exponential?
24. Define diode?
25. What are the characterstics of diode?
26. Draw the ideal characteristics of P-N junction diode?
27. What is the diode characterstics?

28. What is the break down voltage in diode?
29. What is the effect of PN junction diodes?
30. What is PVI?

Experiment No. 2

Examine the reverse bias characteristics of a Zener diode and demonstrate its application as a voltage regulator under varying conditions.

AIM:

Plot the V-I characteristics of a Zener diode, find zener breakdown voltage in reverse bias condition and perform Zener diode voltage regulator.

APPARATUS:

S.No	Apparatus	Type	Range	Quantity
01	Zener diode	IMZ5.1V		01
02	Resistance		470Ω	01
03	Regulated Power supply		(0-30V)	01
04	Ammeter		(0-100mA)	02
05	Voltmeter		(0-10V)	01
06	Decade Resistance Box		(0-10K)	01
07	Bread board and Wires			

THEORY:

A zener diode is heavily doped p-n junction diode, specially made to operate in the break down region. A p-n junction diode normally does not conduct when reverse biased. But if the reverse bias is increased,at a particular voltage it starts conducting heavily.This voltage is called Break down Voltage. High current through the diode can permanently damage the device.

To avoid high current, we connect a resistor in series with zener diode. Once the diode starts conducting it maintains almost constant voltage across the terminals whatever may be the current through it, i.e., it has very low dynamic resistance. It is used in voltage regulators.

CIRCUIT DIAGRAM:

Reverse Biased Zener diode:

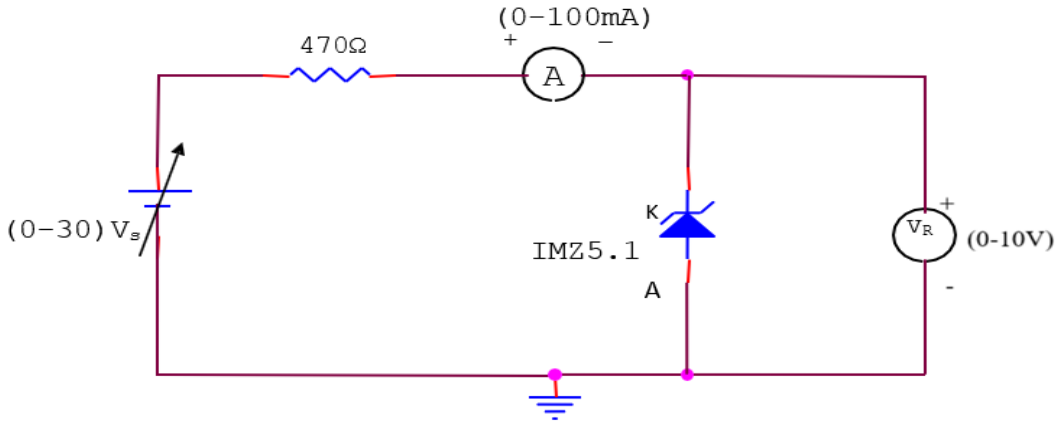


Figure 2.1: Reverse Biased Zener diode:

Zener diode as shunt Voltage Regulator:

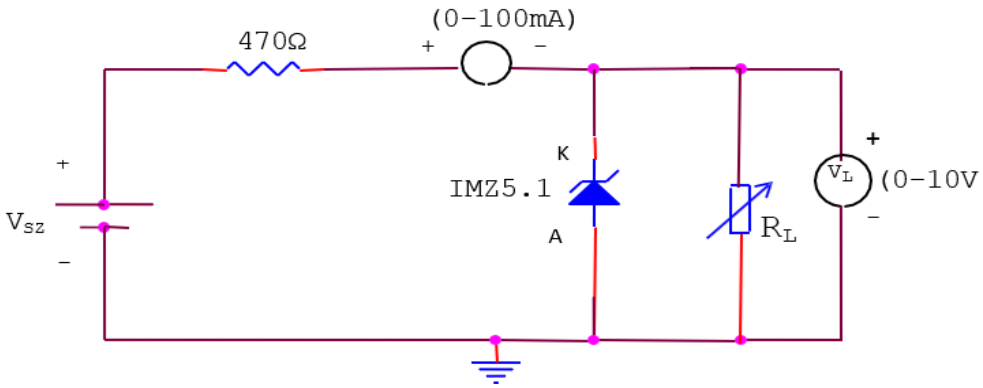


Figure 2.2: Zener diode as shunt Voltage Regulator:

PROCEDURE:

1. Connect the Zener diode in Reverse bias i.e; anode is connected to negative of the power supply and cathode is connected to positive of the power supply as in circuit.

2. Vary the input voltage in steps of 1V and note down reverse voltage (VR)and the corresponding values of reverse current (I_R).

3. Plot the graph between reverse voltage (V_R) and the reverse current (I_R).

To plot the load regulation characteristics of the Zener voltage regulator:

1. Connect the Zener diode in Reverse bias i.e; anode is connected to negative of the power supply and cathode is connected to positive of the power supply as in circuit.

2. In finding load regulation, input voltage (Vsz) is kept constant i.e source voltage is chosen as a voltage at which Zener voltage V_Z is remaining constant while the current is increasing (Vsz from 1st circuit characteristics)

3. MeasureV_{NL}(Noloadvoltage) by opening the load resistance.

4. Connect the load resistance, and vary the load resistance from 1100Ω to 100Ωin steps of 100Ω and note down the readings ofV_L and I_Z

5. Calculate % Regulation by using the formula given below.

$$\%\,Regulation = \frac{V_{NL} - V_L}{V_{L/}} X100$$

OBSERVATION TABLE:

1. To plotV-I characteristics

S.No	V_s(V)	V_R(V)	I_R(mA)

2. Find load regulation characteristics

V_{NL}= ----------

S.No	R_L	I_Z(mA)	V_L(V)	%Regulation
	1100 **To** **100** (insteps of 100)			

Note: Keeping the input voltage constant if the load resistance is increased zener current increases so as to make the load voltage to remain constant.

EXPECTED GRAPH:

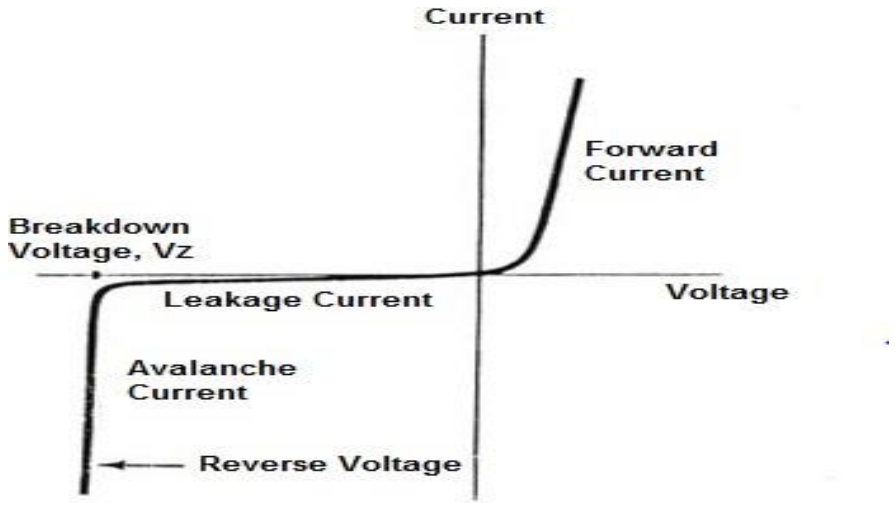


Figure 2.3: Expected wave form Zener Diode Characteristics

RESULT: Thus, the V–I characteristics of a Zener diode under forward and reverse bias are studied and plotted.

REALTIME APPLICATIONS:

1.Voltage Regulation
Used in power supplies to maintain a constant output voltage despite changes in input voltage or load.

2. Overvoltage Protection
Protects electronic circuits from damage by limiting excess voltage.

3. Voltage Reference Circuits
Provides a fixed reference voltage in operational amplifiers, ADCs, and DACs.

4. Surge and Transient Protection
Protects circuits from sudden voltage spikes caused by lightning or switching.

5. Clipping Circuits
Used to limit the maximum voltage level of a signal.

6. Clamping Circuits
Helps shift voltage levels in waveform shaping applications.

7. Meter Protection
Protects voltmeters and measuring instruments from overload.

8. Switching Circuits
Used as a voltage-controlled switch in electronic circuits.

9. Automotive Electronics
Protects ECUs and sensors from voltage fluctuations.

10. Battery Chargers and UPS Systems
Maintains safe voltage levels during charging and power backup.

VIVA QUESTIONS:

1. What is a Zener diode?
2. Who invented the Zener diode?
3. What is meant by Zener breakdown?
4. In which region does a Zener diode normally operate?
5. What is the symbol of a Zener diode?
6. What is the typical voltage range of Zener diodes?
7. What is meant by Zener voltage (Vz)?
8. How is a Zener diode different from a normal PN Junction Diode?
9. Why is a Zener diode heavily doped?
10. What happens when the applied voltage exceeds the Zener voltage?
11. Why is the Zener diode used in reverse bias?
12. What is the difference between Zener breakdown and Avalanche Breakdown?
13. What is the V-I characteristic of a Zener diode?
14. Why is a resistor connected in series with a Zener diode?
15. What is the main application of a Zener diode?
16. How does a Zener diode work as a voltage regulator?
17. Where are Zener diodes commonly used in electronic circuits?
18. Can a Zener diode be used as a voltage reference? Explain.
19. What happens if the current through the Zener diode exceeds its maximum rating?
20. What factors affect the Zener voltage?
21. How do you select a Zener diode for a voltage regulator circuit?
22. What is the power rating of a Zener diode?
23. Explain the working principle of a Zener voltage regulator circuit.
24. What are the advantages and limitations of Zener diode regulators?
25. How do you experimentally determine the Zener voltage?
26. How does temperature affect Zener diode operation?
27. What is the difference between Zener diode regulator and transistor regulator?

28. What precautions should be taken while using a Zener diode in a circuit?
29. What is dynamic resistance of a Zener diode?
30. Draw and explain the V-I characteristics of a Zener diode.

Experiment No. 3

Design and analyze half-wave and full-wave rectifiers (centre-tap) with and without capacitor filters to evaluate ripple factor and output voltage.

HALF-WAVE RECTIFIER

AIM: To rectify the AC signal and to determine the ripple factor and percentage of regulation of a half-wave rectifier with and without a capacitor filter.

APPARATUS:

S.No	Apparatus	Type	Range	Quantity
01	Transformer	Center tapped	12-0-12V	01
02	Diode	IN4007		02
03	Resistance		1KΩ	01
04	Capacitor		1000µF/25V	01
05	Multimeter		(0-20V)	01
06	CRO			01
07	Breadboard and Wires			

Theory:

A device that converts a sinusoidal input waveform into a unidirectional waveform with a non-zero average component is called a **rectifier**.

A practical **half-wave rectifier** with a resistive load is shown in the circuit diagram. During the positive half-cycle of the input, the diode conducts and the entire input voltage appears across the load resistance R_L.During the negative half-cycle, the diode is reverse biased and behaves like an open circuit; hence, the output voltage is zero. The filter used is a capacitor connected from the rectifier output to ground. The capacitor charges quickly during the rising portion of the input

voltage and discharges slowly through R_L after the positive peak. The variation in the capacitor voltage due to this charging and discharging is called **ripple voltage.** Since ripple is undesirable, smaller ripple indicates better filtering action.

A **full-wave rectifier** consists of two half-wave rectifiers connected to a common load. One rectifies during the positive half-cycle of the input, while the other rectifies during the negative half-cycle. The transformer supplies the two diodes (D1 and D2) with sinusoidal voltages that are equal in magnitude but opposite in phase. During the positive half-cycle, diode D1 conducts and diode D2 remains OFF. During the negative half-cycle, diode D1 is OFF and diode D2 conducts. As in the half-wave rectifier, ripple is undesirable, and better filtering is achieved by reducing the ripple content.

CIRCUIT DIAGRAM:

WITHOUT FILTER:

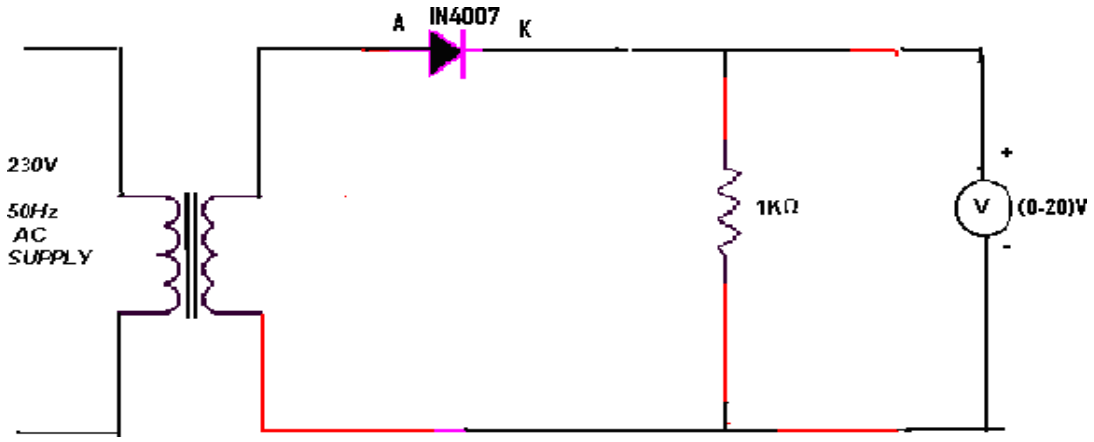


Figure 3.1: Circuit Diagram of Half Wave Rectifier without Filter

WITH FILTER:

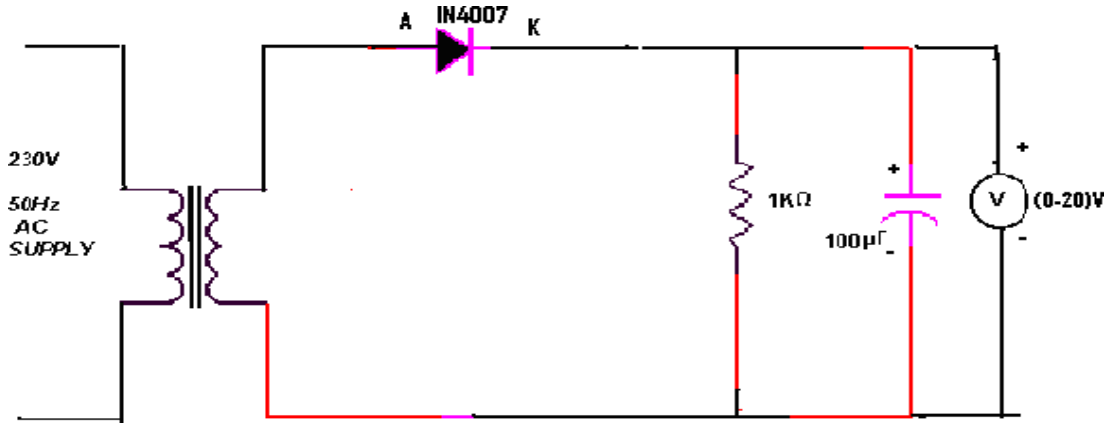


Figure 3.2: Circuit Diagram of Half Wave Rectifier with Filter

CALCULATIONS:

Theoretical calculations for Ripple factor of Half wave Rectifier: -

Without Filter:

$$V_{dc} = V_m/\pi$$

$$V_{rms} = V_m/2$$

$$\text{Ripple factor} = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1} \qquad = 1.21$$

With Capacitor Filter:

$$\text{Ripple factor} = \frac{1}{2\sqrt{3}\,fCR_L}$$

Where f =50Hz
C =1000μF
R_L=1KΩ

PROCEDURE:

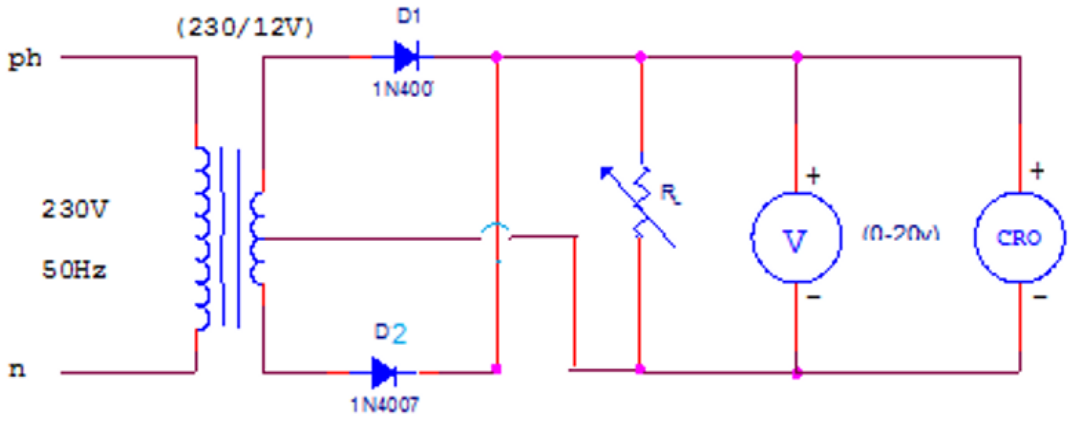
HWR Without Filter:

1. Connections are made as per the circuit diagram of the rectifier with out filter.
2. Connect the primary side of the transformer to ac mains and the secondary side to the rectifier input.
3. Note down the no load voltage before applying the load to the Circuit and by using the Multimeter, measure the ac input voltage of the rectifier and its frequency.
4. Now Vary the R_L insteps of 100Ω by varying the DRB from 1100Ω to 100Ω and note down the load voltage (V_L) using the multimeter for each value of R_L and calculate the percentage regulation.
5. Measure the AC and DC voltage at the output of the rectifier for each value of R_L using Multimeter.
6. Now Observe the output wave form on CRO across R_L and find out value of V_m.
7. Now calculate V_{dc}, V_{rms}, Ripple Factor and other parameters of halfwave rectifier according to the given formulae.
8. Measure the amplitude and time period of the transformer secondary(inputwaveform)by connecting CRO.
9. Feed the rectified output voltage to the CRO and measure the time period and amplitude of the waveform.

HWR with Capacitor Filter:

1. Connections are made as per the circuit diagram of the rectifier with filter.
2. Connect the primary side of the transformer to the AC mains and the secondary side to the rectifier input.
3. Using a multimeter, measure the AC input voltage of the rectifier and the AC and DC voltages at the rectifier output.
4. Measure the amplitude and time period of the transformer secondary (input waveform) by connecting the CRO.
5. Feed the rectified output voltage to the CRO and measure the amplitude and time period of the output waveform.

Full wave Rectifier without Filter



Full wave Rectifier with capacitor Filter

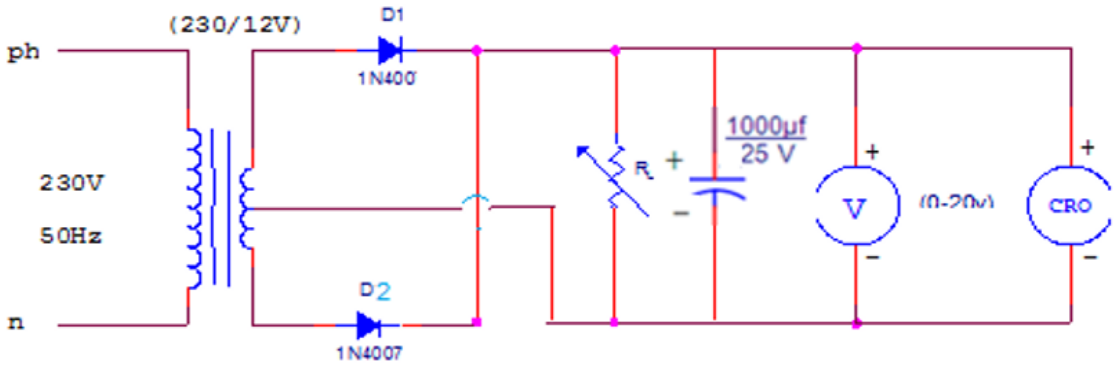


Figure 3.3: FWR with and Without Filter

Theoretical calculations for Ripple factor of Full wave Rectifier: -

Without Filter: -

$$V_{dc} = \frac{2V_m}{\pi}$$

$$V_{rms} = \frac{V_m}{\sqrt{2}}$$

$$\text{Ripple factor} = \sqrt{\left(\frac{V_{rms}}{V_{dc}}\right)^2 - 1} \qquad = 0.482$$

With Capacitor Filter:

$$\text{Ripple factor} = \frac{1}{4\sqrt{3}fCR_L}$$

Where f =50Hz
C =1000µF
R_L=1KΩ

PROCEDURE:

FWR Without Capacitor Filter:

1. Connections are made as per the circuit diagram of the rectifier without filter.
2. Connect the primary side of the transformer to the AC mains and the secondary side to the rectifier input.
3. By the multimeter, measure the ac input voltage of the rectifier and, ac and dc voltage at the output of the rectifier.
4. Measure the amplitude and time period of the transformer secondary (input wave form) by connecting the CRO.

5. Feed the rectified output voltage to the CRO and measure the time period and amplitude of the Waveform.

FWR with Capacitor Filter:

1. Connections are made as per the circuit diagram of the rectifier with filter.
2. Connect the primary side of the transformer to ac mains and the secondary side to the rectifier input.
3. By the multimeter, measure the ac input voltage of the rectifier and, ac and dc voltage at the output of the rectifier.
4. Measure the amplitude and time period of the transformer secondary(input waveform) by connecting CRO.
5. Feed the rectified output voltage to the CRO and measure the time period and amplitude of the waveform.

OBSERVATION TABLE:

HWR without Filter:

R_L (Ω)	V_L(V)	V_m (V)	$V_{dc}=\frac{Vm}{\pi}$ (V)	$V_{rms}=\frac{Vm}{2}$ (V)	$Vr(rms)=\sqrt{Vrms^2-Vdc^2}$ (V)	R.F= $\frac{Vr(rms)}{Vdc}$

HWR With Capacitor Filter:

R_L (Ω)	V_L(V)	V_m(V)	V_r(V)	$Vdc=Vm-\frac{Vr}{2}$ (V)	$Vr(rms)=\frac{Vr}{2\sqrt{3}}$	R.F=$\frac{Vr(rms)}{Vdc}$

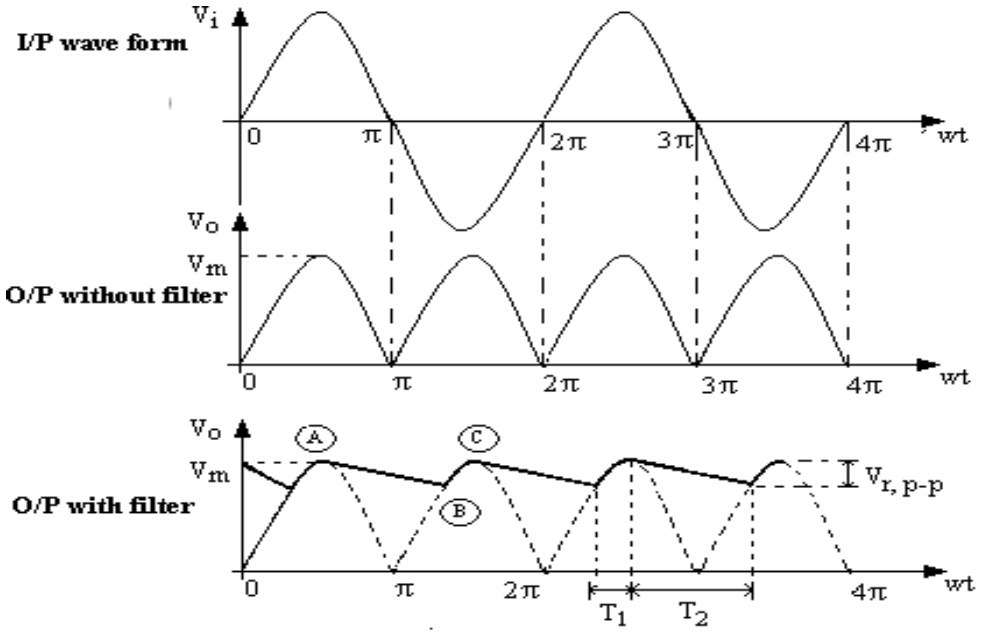
FWR without Filter:

R_L (Ω)	V_L (V)	V_m (V)	$Vdc=\frac{2Vm}{\pi}$ (V)	$Vrms=\frac{Vm}{\sqrt{2}}$ (V)	$Vr(rms)=\sqrt{Vrms^2-Vdc^2}$ (V)	R.F=$\frac{Vr(rms)}{Vdc}$	%Regulation $=\frac{V(NL)-V(L)}{VL}$

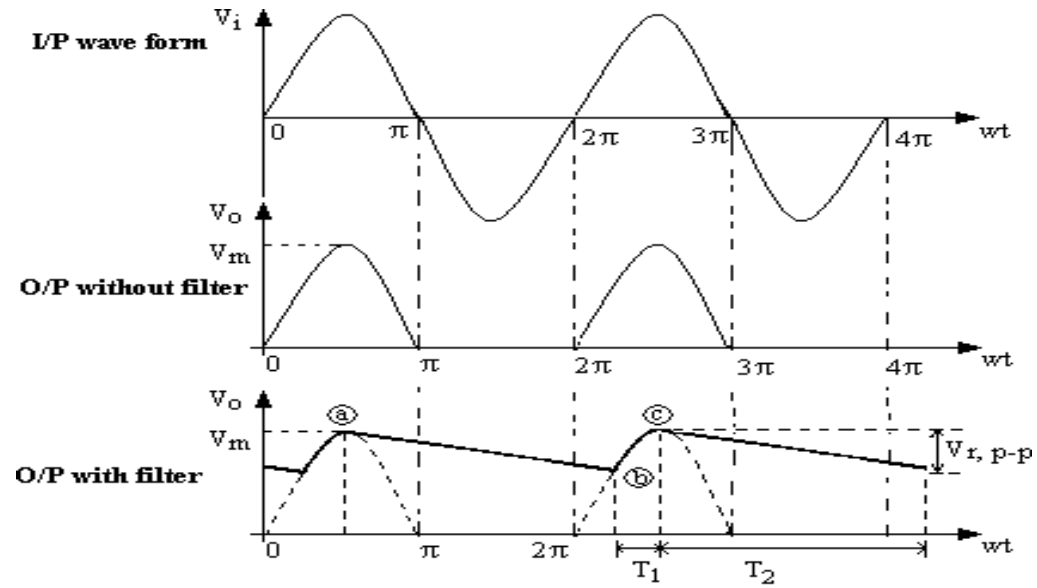
FWR with capacitor filter:

R_L (Ω)	V_L (V)	V_m (V)	V_r(V)	$V_{ac}=V_m-V_r/2$ (V)	$Vr(rms)=\frac{Vr}{4\sqrt{3}}$	R.F=$\frac{Vr(rms)}{Vdc}$	%Regulation $=\frac{V(NL)-V(L)}{VL}$

EXPECTED WAVE FORMS:



Full-wave Rectifier with capacitor filter wave form



Half-wave Rectifier with capacitor filter wave form

RESULT: The input and output wave forms of half wave rectifier and full wave rectifier are is plotted.

Ripple factor of HWR without filter =

Ripple factor of HWR with capacitor filter =

Ripple factor of FWR without filter =

Ripple factor of FWR with capacitor filter =

REALTIME APPLICATIONS:

1. Power Supplies (AC to DC Conversion)

Used in TVs, computers, mobile chargers, laptops

Converts AC mains supply into DC required by electronic circuits

2. Battery Charging Circuits

Used in mobile phones, UPS, inverters, electric vehicles

Rectifier converts AC into DC to charge batteries safely

3. DC Motor Drives

Used in electric trains, cranes, lifts, rolling mills

Rectifiers supply controlled DC voltage to DC motors

4. Radio and Communication Systems

Used in AM radio receivers

Detects and converts modulated AC signals into audio signals

5. Electroplating and Electrolysis

Used in gold plating, silver plating, metal purification

Requires DC supply obtained using rectifiers

6. Welding Equipment

Used in arc welding machines

Rectifiers convert AC to high-current DC for stable welding

7. Uninterruptible Power Supply (UPS)

Used in hospitals, data centers, computers

Rectifier charges battery and supplies DC to inverter

8. HVDC Transmission Systems

Used in long-distance power transmission

Rectifiers convert AC to DC at sending end

9. X-Ray Machines

Used in medical imaging

Rectifier converts AC into high-voltage DC

10. Signal Demodulation

Used in communication receivers

Rectifier extracts information signal from carrier wave

VIVA QUESTIONS:

1. What is a rectifier?
2. What is a Half-Wave Rectifier?
3. What is a Full-Wave Rectifier?
4. What is the main function of a rectifier circuit?
5. Which device is mainly used in rectifier circuits?
6. What is the role of a PN Junction Diode in a rectifier?
7. What type of input supply is given to a rectifier?
8. What type of output is obtained from a rectifier?
9. How many diodes are used in a Half Wave Rectifier?
10. During which half cycle does a Half Wave Rectifier conduct?
11. What happens during the negative half cycle in HWR?
12. What is the ripple frequency of a Half Wave Rectifier?
13. What is the efficiency of a Half Wave Rectifier?
14. What are the disadvantages of a Half Wave Rectifier?
15. How many diodes are used in a center-tapped Full Wave Rectifier?
16. How many diodes are used in a bridge Full Wave Rectifier?
17. What is the ripple frequency of a Full Wave Rectifier?
18. What is the efficiency of a Full Wave Rectifier?
19. Why is a Full Wave Rectifier more efficient than a Half Wave Rectifier?
20. What is the function of a center-tapped transformer in FWR?
21. What is ripple factor in a rectifier?
22. What is Peak Inverse Voltage (PIV) of a diode?
23. Compare the PIV of HWR and FWR.
24. What is the Transformer Utilization Factor (TUF)?
25. What is the output frequency of HWR and FWR?
26. Why are filters used in rectifier circuits?
27. What is the purpose of a filter capacitor in a rectifier?

28. Which rectifier produces less ripple?
29. Why is the bridge rectifier widely used in power supplies?
30. What are the applications of rectifier circuits in electronic devices?

Experiment No. 4

Implement clipper and clamper circuits to observe waveform shaping through positive, negative, and biased configurations.

AIM: To study the clipping circuits for different reference voltages and to verify their responses.

APPARATUS:

1. Resistors- 1KΩ
2. IN4007Diode–2No.
3. Breadboard.
4. CRO(1Hz–20MHz)
5. Function Generator(1Hz-1MHz)
6. Power supply(0-30V)
7. Connecting wires.

THEORY:

A non-linear semiconductor diode in combination with a resistor can function as a clipper circuit. Energy-storage components are not required in the basic process of clipping. These circuits select a portion of an arbitrary waveform that lies above or below a particular reference voltage level, and the selected portion of the waveform is used for transmission. Hence, they are also referred to as **voltage limiters, current limiters, amplitude selectors, or slicers**.

There are three different types of clipping circuits:

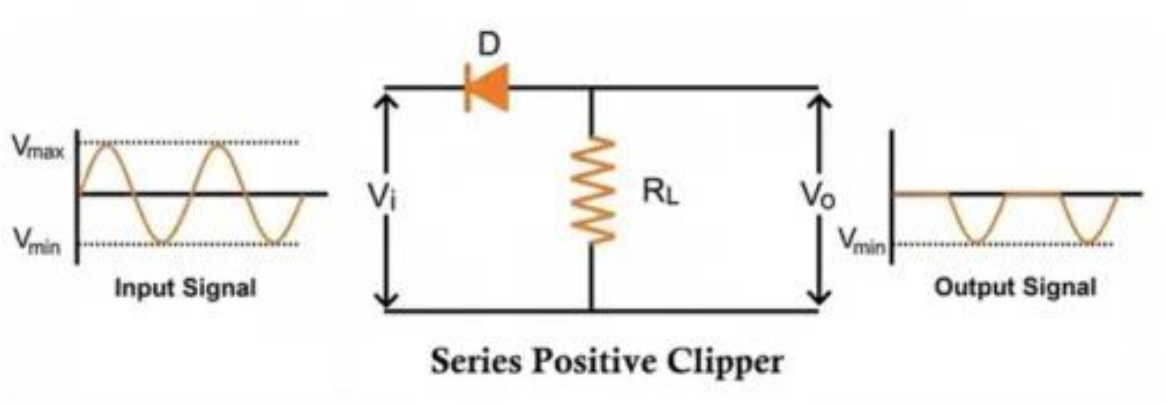
1. **Positive clipping circuit**
2. **Negative clipping circuit**
3. **Positive and negative clipping circuit (slicer)**

In a **positive clipping circuit**, the positive portion of the sinusoidal signal is clipped, and only the negative portion appears at the output. When a reference voltage is added, instead of clipping the entire positive cycle, only the portion of the positive cycle that exceeds the reference voltage level is clipped.

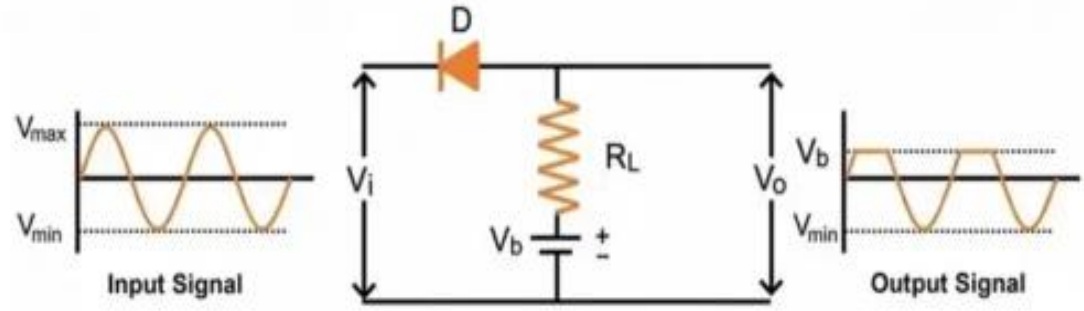
In a **negative clipping circuit**, the negative portion of the sinusoidal signal is clipped, while the positive portion appears at the output.

CIRCUIT DIAGRAM:

SERIES POSITIVE CLIPPER WITH AND WITHOUT BIAS:



Series Positive Clipper



Series Positive Clipper with Positive Bias

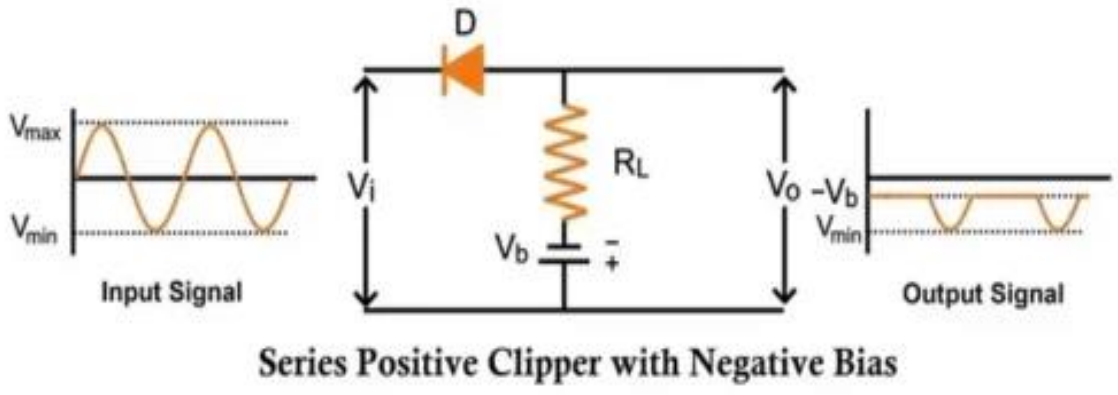
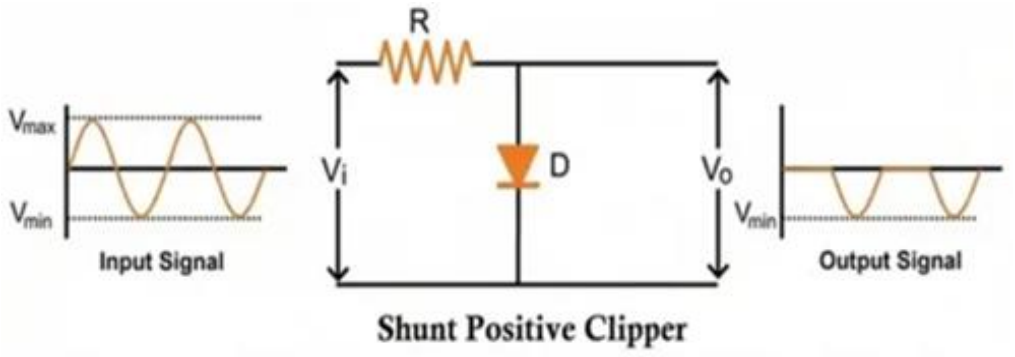
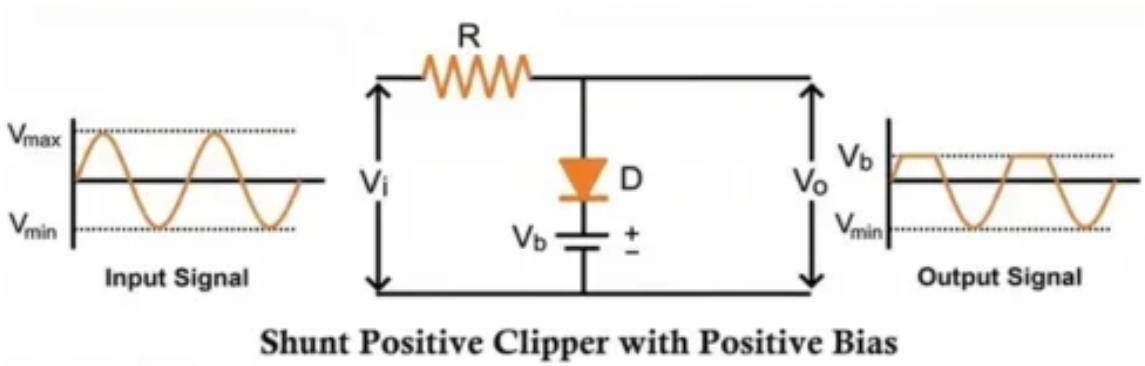


Figure 4.1: Series Positive Clipper With And Without Bias

SHUNT POSITIVE CLIPPER WITH AND WITHOUT BIAS:





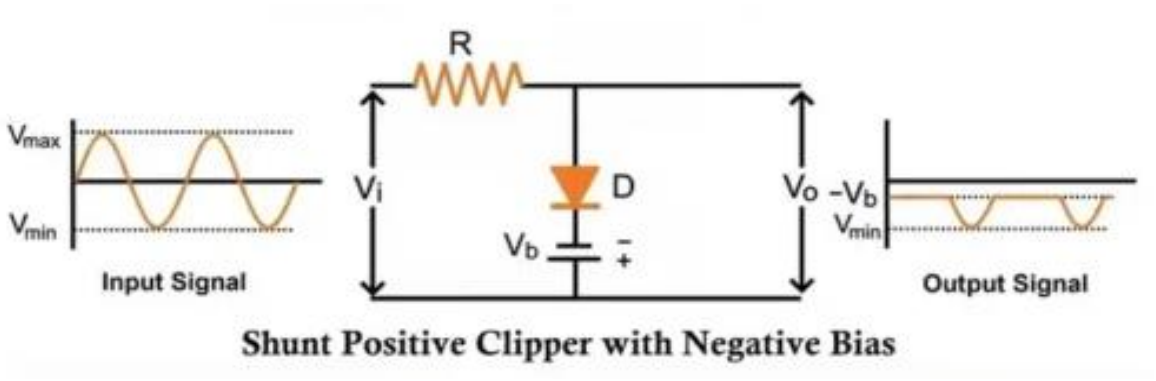
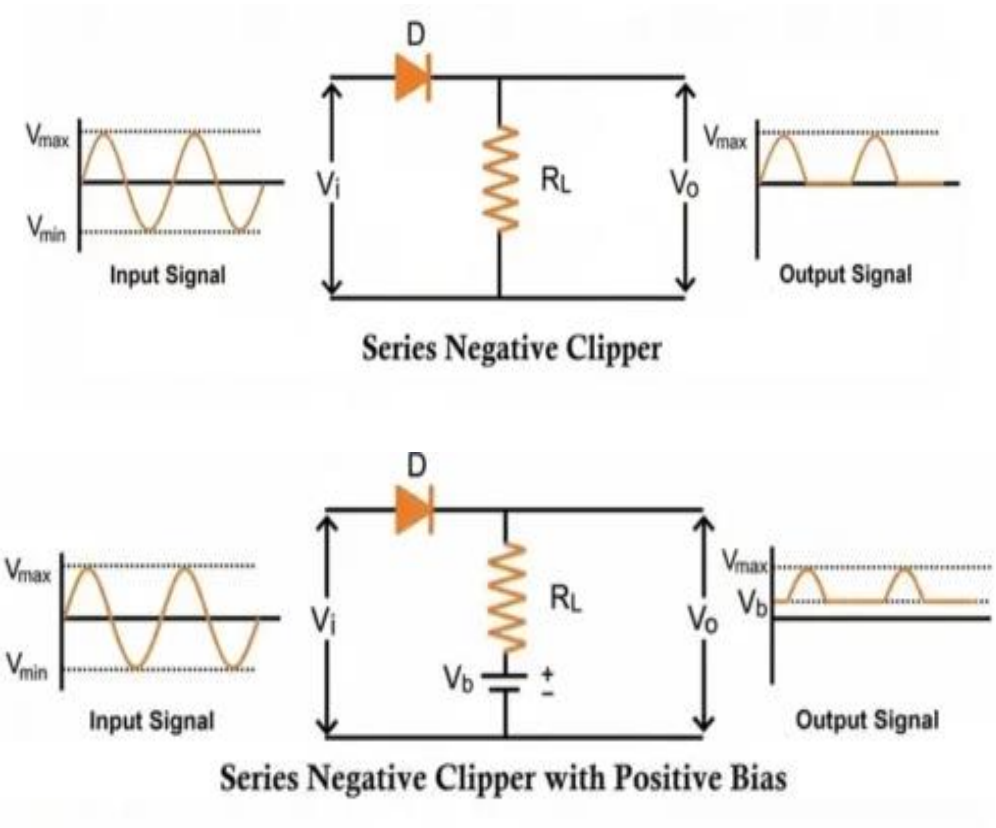


Figure 4.2: Shunt Positive Clipper With And Without Bias

SERIES NEGATIVE CLIPPER WITH AND WITHOUT BIAS:



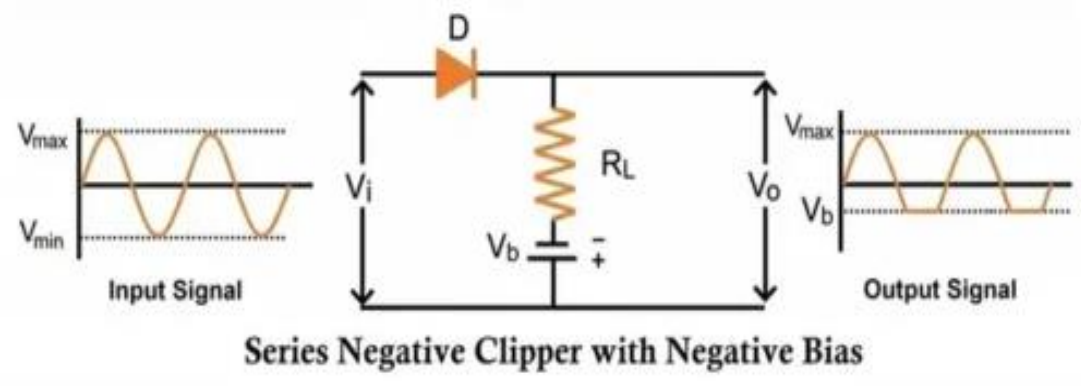
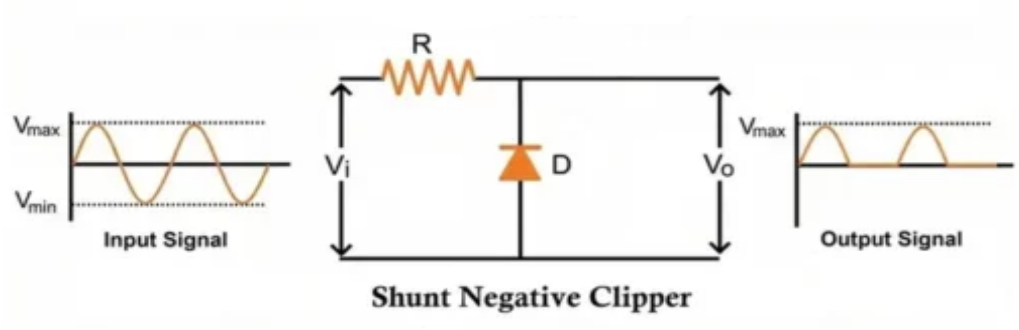
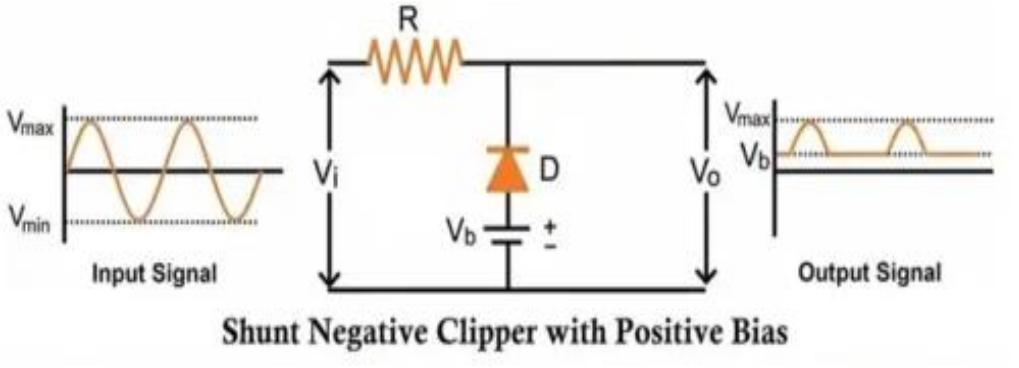


Figure 4.3: Series Negative Clipper With And Without Bias

SHUNT NEGATIVE CLIPPER WITH AND WITHOUT BIAS:





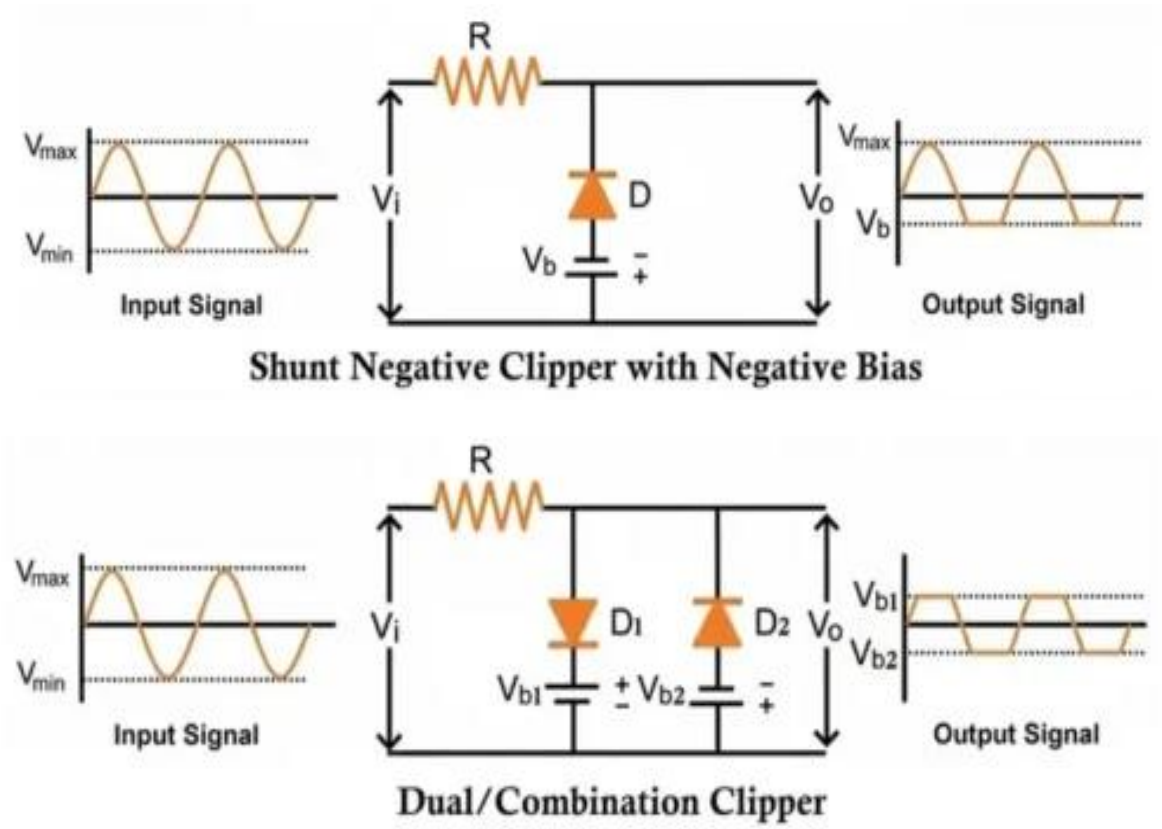


Figure 4.4: Shunt Negative Clipper With And Without Bias

Negative Clipper:

For $V_i < V_R + V_r$, the diode **D** is **OFF** since it is reverse biased and hence does not conduct. As no current flows, there is no voltage drop across the resistor **R**. Therefore,

$$V_o = V_i \quad \text{for } V_i < V_R + V_r$$

where V_r is the **cut-in (threshold) voltage** of the diode.

For $V_i > V_R + V_r$, the diode **D** is **ON** since it is forward biased and the potential barrier is overcome. Hence, the output voltage is limited to

$$V_o = V_R + V_r$$

Transfer Characteristic Equation:

$$V_o = \begin{cases} V_i, & \text{for } V_i < V_R + V_r \\ V_R + V_r, & \text{for } V_i > V_R + V_r \end{cases}$$

Positive Clipper:

When $V_i > V_R + V_r$, the diode is forward biased and conducts. Since the diode is **ON**, it behaves like a short circuit, and therefore,

$$V_o = V_R + V_r$$

When $V_i < V_R + V_r$, the diode is reverse biased and hence **OFF**. It acts as an open circuit, and therefore,

$$V_o = V_i$$

Transfer Characteristic Equation:

$$V_o = \begin{cases} V_i, & \text{for } V_i < V_R + V_r \\ V_R + V_r, & \text{for } V_i > V_R + V_r \end{cases}$$

PROCEDURE:

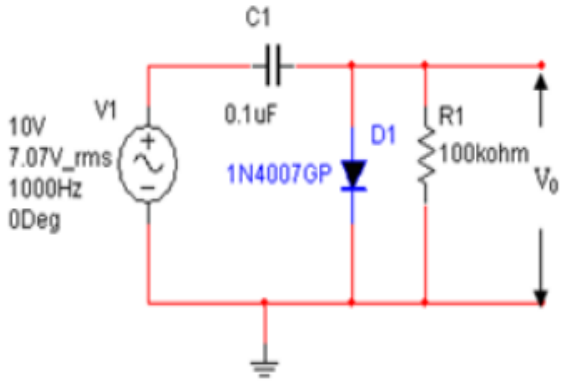
1. Connect the circuit as shown in the figures.
2. In each case, by applying different value of reference voltage change the peak voltage of input signal and note the theoretical and practical clipping values.
3. Observe the Output waveform (V_O in the circuit) on the CRO and compare it with theoretical values.
4. Sketch the Input as well as Output waveforms and mark the voltage levels.
5. Obtain the transfer characteristics of Clipper circuit, by keeping CRO in X-Y mode.

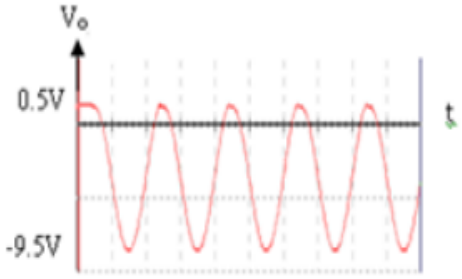
OBSERVATION TABLE:

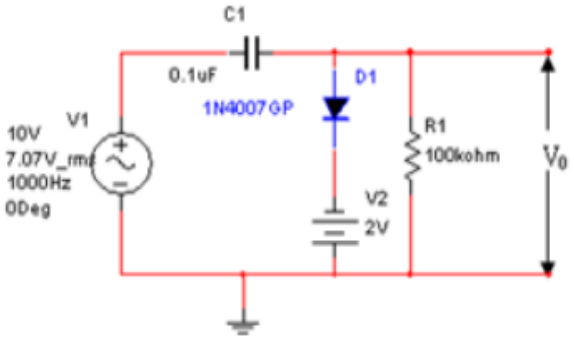
Name Of the Clipper	**Negative Clipper**		**Positive Clipper**		**2-Level Clipper**	
Wave Form	I/P	O/P	I/P	O/P	I/P	O/P
Amplitude(p-p)in volts						
Time Period (mSec)						

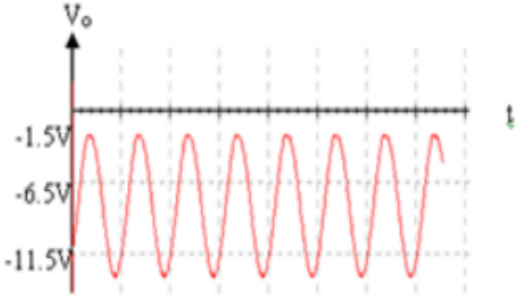
CLAMPERS:

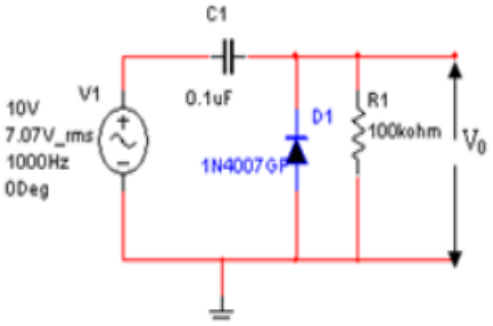
CIRCUIT DIAGRAM **O/P WAVEFORMS**

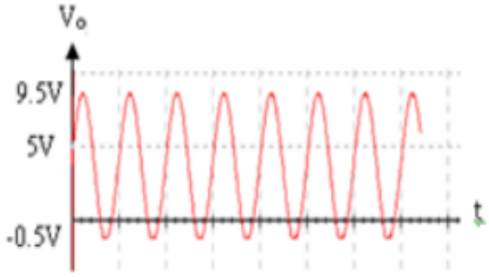












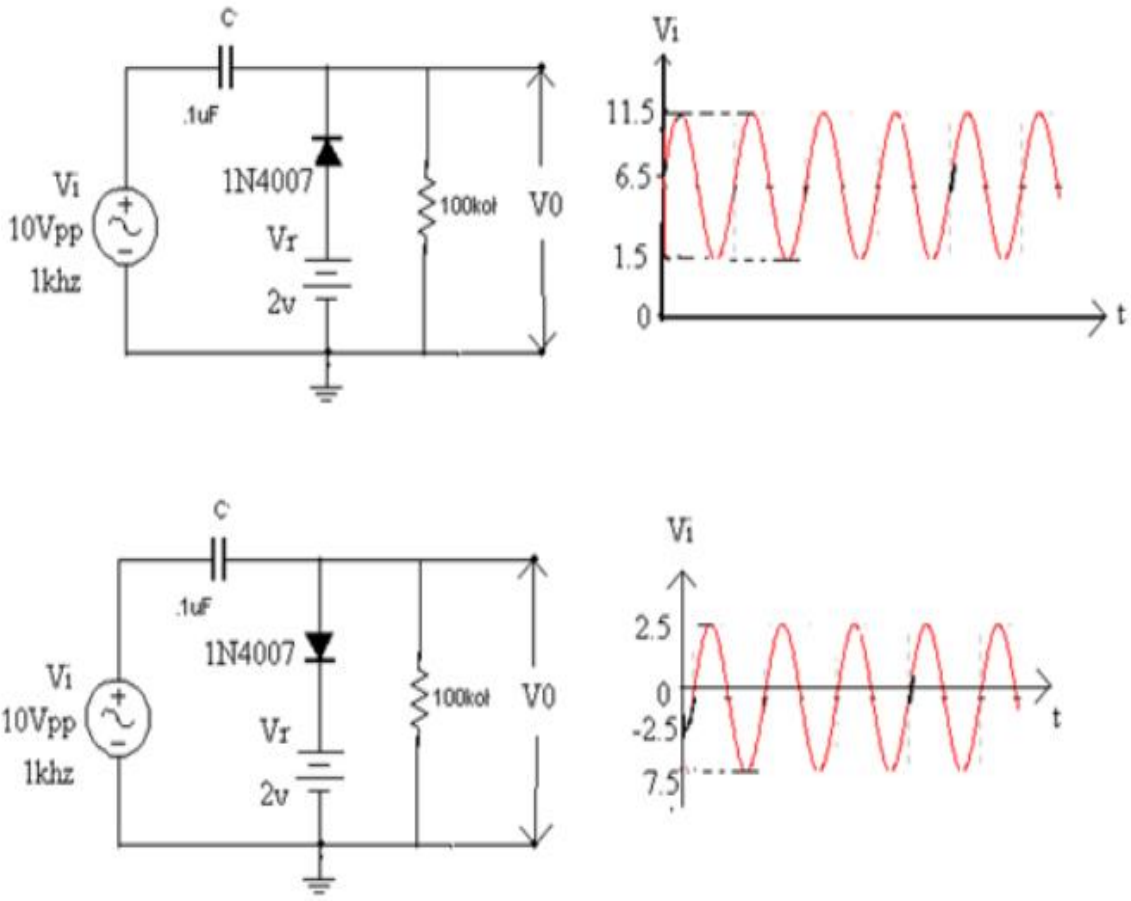


Figure 4.5: Clampers

RESULT:

Thus, Different types of Clippers and clamping circuits are studied and observed the response for different combinations of V_R and diodes.

REAL-TIME APPLICATIONS OF CLIPPERS:

Clippers are used to remove or limit unwanted portions of a signal without distorting the remaining part. In real-time applications, they are used in wave-shaping circuits to protect electronic devices from voltage spikes by limiting peak voltage levels. Clippers are commonly used in TV and radio receivers to remove noise, in signal processing circuits to extract information signals, and in over-voltage protection circuits for sensitive components. They are also used in digital circuits to produce square waveforms from sinusoidal inputs, making them essential in pulse shaping and logic circuits.

REAL-TIME APPLICATIONS OF CLAMPERS:

Clampers are used to shift the DC level of a waveform without changing its shape. In practice, they are used in television and video circuits to restore the required DC level of video signals. They are also applied in communication systems to adjust signal levels, in oscilloscope circuits to display signals above or below the reference level, and in analog signal processing where waveform translation is required. Clampers are widely used in pulse circuits, voltage level shifters, and AC signal conditioning.

VIVA QUESTIONS:

1. What is a clipper circuit?
2. What is the main function of a clipper?
3. What are the types of clippers?
4. What is a series clipper?
5. What is a shunt (parallel) clipper?
6. How does a positive clipper work?
7. How does a negative clipper work?
8. What is the effect of adding a bias voltage in a clipper?
9. What are the practical applications of clippers?
10. Can clippers be used with AC and DC signals?
11. What is the difference between a biased and unbiased clipper?
12. What happens when a diode in a clipper is reversed?
13. What is the voltage level at which clipping occurs?
14. How can you change the clipping level?
15. Why are clippers called “limiter circuits”?
16. What is a clamper circuit?
17. What is the main function of a clamper?
18. What is the difference between a clipper and a clamper?
19. What are the types of clamper circuits?
20. What is a positive clamper?
21. What is a negative clamper?
22. How does a capacitor work in a clamper circuit?
23. What is the effect of adding a DC bias in a clamper?
24. What are the practical applications of clampers?
25. Can a clamper shift an AC waveform up or down?
26. What is the difference between series and shunt clamper?
27. How do you choose the capacitor and resistor values in a clamper?
28. Why is a diode used in a clamper circuit?
29. What is the output voltage level of a positive clamper?
30. How can a clamper be used in TV and signal processing circuits?

Experiment No. 5

Plot the input and output characteristics of a BJT in common emitter configuration to determine input/output resistance current gain.

AIM:

1. To study the input and output characteristics of transistor (BJT) connected in common Emitter configuration.
2. To calculate current gain β.
3. To calculate input resistance Ri & output resistance Ro.

APPARATUS:

S. No	Device	Range/Rating	Qty
1	Regulated DC supply voltage (RPS)	0-30V	1
2	Voltmeter	0-1V or 0-10v,0-20V	1
3	Ammeter	0-10mA,200mA	1
4	Connecting wires & bread board	As required	
5	Transistor BC 107 or 2n2222 or BC547	NPN	1
6	Resistor	1K,100K	1

THEORY:

A transistor is a three-terminal device. The terminals are emitter, base, collector. In common emitter configuration, input voltage is applied between base and emitter terminals and output is taken across the collector and emitter terminals. Therefore, the emitter terminal is common to both input and output. The input characteristics resemble that of a forward biased diode curve. This is expected since the Base-Emitter junction of the transistor is forward biased. As compared to CB arrangement IB increases less rapidly with VBE. Therefore, input resistance of CE circuit is higher than that of CB circuit. The output characteristics are drawn between Ic and VCE at constant IB. the collector current varies with VCE unto few volts only. After this the collector current becomes almost constant, and independent of VCE. The value of VCE up to which the collector current changes with V CE is known as Knee voltage. The transistor always operated in the region above Knee voltage, IC is always constant and is approximately equal to IB.

The current amplification factor of CE configuration is given byB = ΔIC/ΔIB

CIRCUIT DIAGRAM:

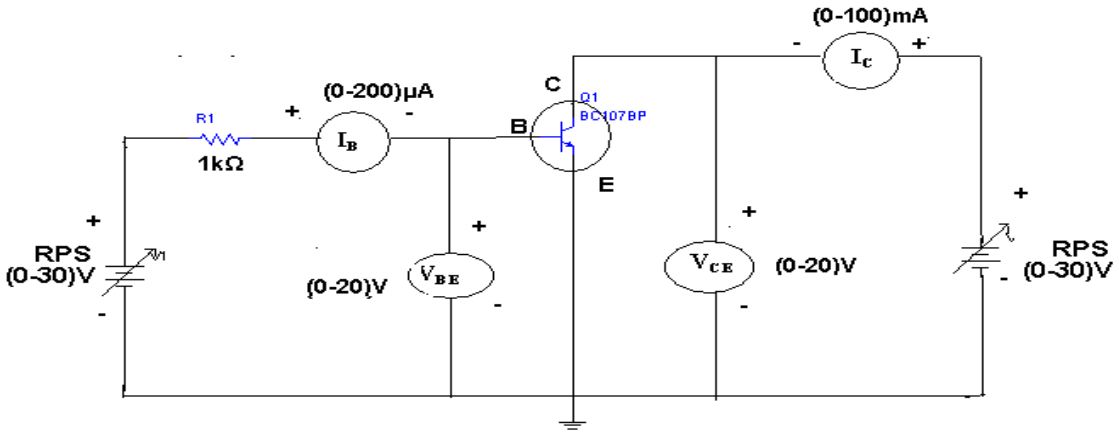


Figure 5.1: Input and Output Characteristics of a CE

PROCEDURE:

Input characteristics:

1. Connect the circuit according to the circuit diagram of input characteristics
2. Keep (Collector to Emitter Voltage) VCE=0V) by varying VCC (collector supply voltage). Increasing VBB (Base supply Voltage from 0 onwards (0.1V, 0.2V….0.75V) observe IB (Base current) for different values of VBE (Base to Emitter voltage).
3. Repeat the Step 2 for Different (collector to Emitter voltage) VCE i.e. 3V & 6V.
4. Tabulate the results in the tabular form and plot the graph.

Output characteristics:

1. Connect the circuit according to the circuit diagram of output characteristic.
2. Keep (collector supply voltage) VCC=0V. Increase (Base supply Voltage) VBB to get Base current IB= 3μA.
3. Now increase (Collector supply voltage) VCC from 0 onwards and observe the Collector current IC for different Values of (Collector to Emitter voltage) VCE Without exeding the rated value (IC=15mA)
4. Tabulate the results in the tabular coloum and plot the graph

OBSERVATIONS:

INPUT CHARACTERISTICS:

S.NO	V_{CE} = 1V		V_{CE} = 2V		V_{CE} = 4V	
	V_{BE}(V)	I_B(µA)	V_{BE}(V)	I_B(µA)	V_{BE}(V)	I_B(µA)

OUT PUT CHARACTERISTICS:

S.NO	I_B = 5ma		I_B = 10ma		I_B = 15ma	
	V_{CE}(V)	I_C(mA)	V_{CE}(V)	I_CmA)	V_{CE}(V)	I_C(mA)

EXPECTED GRAPHS:

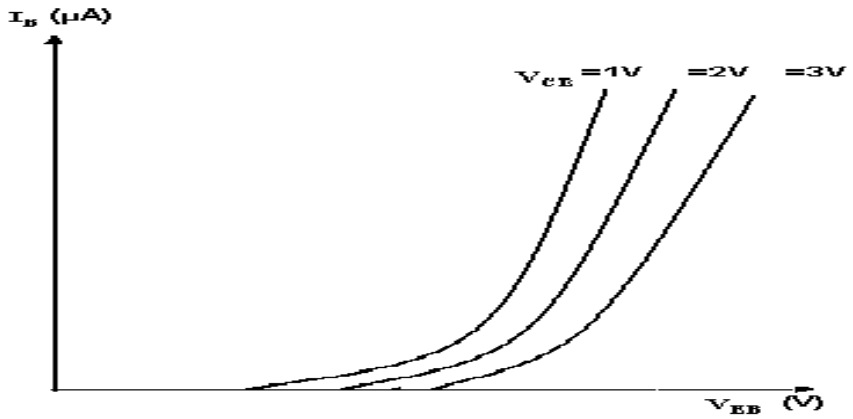


Figure 5.2: Input Characteristics of a CE

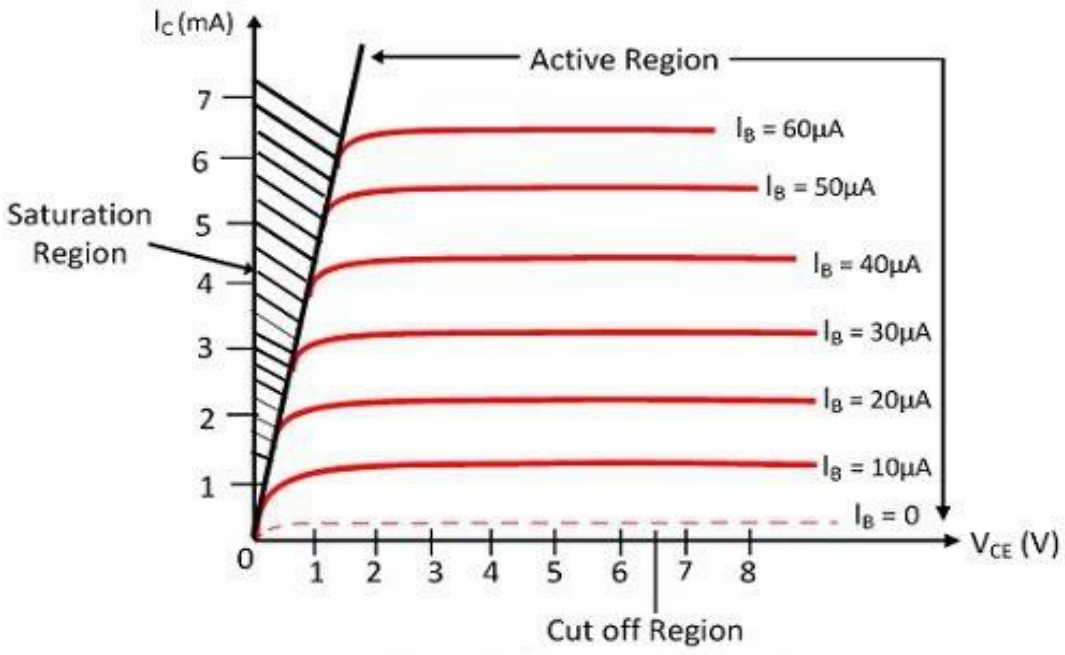


Figure 5.3: Output Characteristics of a CE configuration

RESULT:

The input and output characteristics of CE are observed

REAL-TIME APPLICATIONS:

The Bipolar Junction Transistor (BJT) in common-emitter (CE) configuration is widely used in real-time applications such as audio and **RF amplifiers, electronic switches, oscillators, signal modulation circuits, voltage regulators, and pulse shaping circuits**, because it provides high current, voltage, and power gain. Its input characteristics show the base current (I_B) versus base-emitter voltage (V_{BE}), where the input behaves like a forward-biased diode, while the output characteristics plot collector current (I_C) versus collector-emitter voltage (V_{CE}) for different base currents, showing cut-off, active, and saturation regions. In the active region, $I_C \approx \beta \times I_B$, providing linear amplification, and the output voltage is 180° out of phase with the input, making CE configuration ideal for amplification and switching in practical electronic circuits

Viva Questions:

1. What is Common emitter configuration?
2. What is the range of β for the transistor?
3. What are the input and output impedances of CC configuration?
4. Identify various regions in the output characteristics?
5. What is the relation between α ,β and γ ?
6. Define Cutoff ,Active and Saturation region?
7. Define current gain in CE configuration?
8. Why CE configuration is preferred for amplification?
9. What is the phase relation between input and output?
10. Draw diagram of CE configuration for PNP transistor?
11. What is the power gain of CE configuration?
12. What are the applications of CE configuration?
13. What is a BJT?
14. Why is the Common Emitter configuration widely used?
15. Which junction is forward biased in CE configuration?
16. What is the input of a CE configuration?
17. What is the output of a CE configuration?
18. Define input characteristics of a CE transistor.
19. Define output characteristics of a CE transistor.
20. What is the input resistance of CE configuration?
21. What is the output resistance of CE configuration?
22. What happens to collector current when base current increases?
23. Name the different regions of operation in CE configuration.
24. What is the active region of a transistor?
25. What is saturation region?
26. What is cut-off region?
27. Why CE amplifier provides high voltage gain?
28. What is the role of base current in CE configuration?

29. How is CE different from CB configuration?

30. What is current gain in CE configuration?

Experiment No. 6

Construct and analyze a Common Base (CB) configuration of a BJT to study input-output characteristics and determine current gain (α) and input/output resistance.

AIM:

1. To observe and draw the input and output characteristics of a transistor connected in common base configuration.
2. To find α of the given transistor and also its input and output Resistances.

APPARATUS:

1. Transistor, BC107 -1No.
2. Regulated power supply (0-30V) -1No.
3. Voltmeter (0-20V) - 2No.
4. Ammeters (0-10mA) - 2No.
5. Resistor, 1KΩ - 2No
6. Bread board
7. Connecting wire

THEORY:

A transistor is a three terminal active device. The terminals are emitter, base,collector. In CB configuration, the base is common to both input (emitter) and output(collector). For normal operation, the E-B junction is forward biased and C-B junctionis reverse biased. In CB configuration, I_E is +ve, I_C is –ve and IB is –ve. So

$$\mathbf{V_{EB} = F1\ (V_{CB},\ I_E)\ and}$$
$$\mathbf{I_C = F2\ (V_{EB}, I_B)}$$

With an increasing the reverse collector voltage, the space-charge width at the output junction increases and the effective base width 'W' decreases. This phenomenon is known as "Early effect". Then, there will be less chance for recombination within the base region.With increase of charge gradient with in the base region, the current of minority carriers injected across the emitter junction increases. The current amplification factor of CB configuration is given by,

$$\alpha = \Delta I_C / \Delta I_E$$

Input Resistance,ri = $\Delta V_{BE} / \Delta I_E$ at Constant V_{CB}

Output Résistance, ro = $\Delta V_{CB} / \Delta I_C$ at Constant I_E

CIRCUIT DIAGRAM:

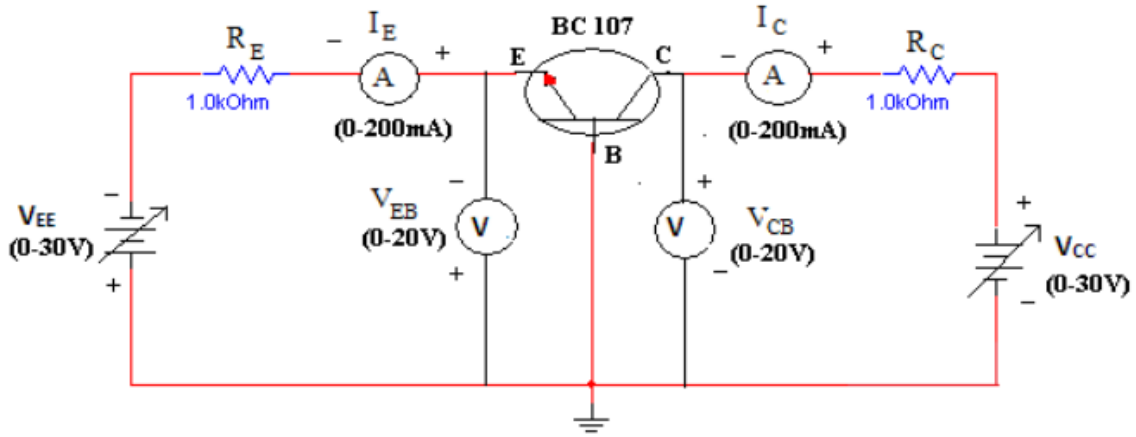


Figure 6.1: Common Base (CB) configuration

MODEL GRAPHS:

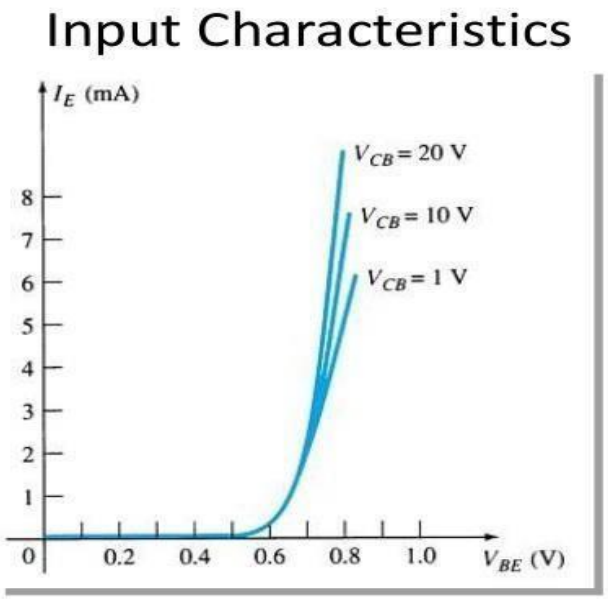


Figure 6.2: Input Characteristics

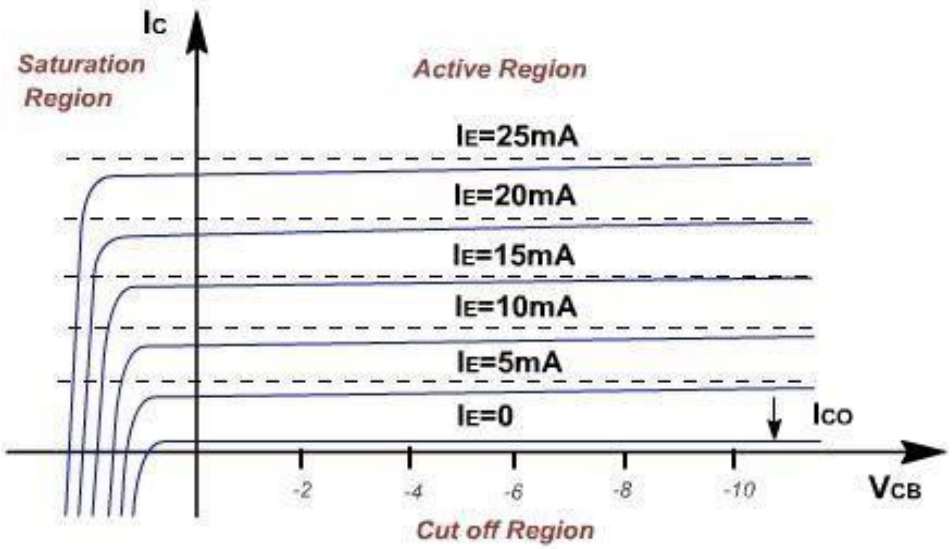


Figure 6.3: Output Characteristics

OBSERVATIONS:

A. INPUT CHARACTERISTICS:

V_{EE}(V)	$V_{CB=}$1V		$V_{CB=}$= 2V		$V_{CB=}$4V	
	V_{EB}(V)	I_E(mA)	V_{EB}(V)	$I_{E(}$mA)	V_{EB}(V)	$I_{E(}$mA)

B. OUTPUT CHARACTERISTICS:

V_{cc}(V)	I_E=10mA		I_E=20mA		I_E=30mA	
	V_{CB}(V)	I_C(mA)	V_{CB}(V)	I_C(mA)	V_{CB}(V)	I_C(mA)

PROCEDURE:

A) INPUT CHARACTERISTICS:

1. Connections are made as per the circuit diagram.
2. For plotting the input characteristics,the output voltage V_{CE} is kept constant at 0V and for different values of V_{EE} note down the values of I_E and V_{BE}
3. Repeat the above step keeping V_{CB} at 2V, 4V, and 6V and all the readings are tabulated.
4. A graph is drawn between$_{EB}$and I_E for constant $V_{CB.}$

B) OUTPUT CHARACTERISTICS:

1. Connections are made as per the circuit diagram.
2. For plotting the output characteristics, the input I_E is kept constant at 0.5mA and for different values of V_{CC}, note down the values of I_C andV_{CB}.
3. Repeat the above step for the values of I_E at1mA,5mA and all the readings are tabulated.
4. A graph is drawn between V_{CB} and Ic for constant I_E

RESULT:

Input and Output characteristics of a Transistor in Common base Configuration are studied and find out the input resistance, output resistance, α.

REALTIME APPLICATIONS:

The common base (CB) configuration of a BJT is mainly used in high-frequency and RF applications because it has low input resistance, high output resistance, and good frequency response**.** In real-time systems, CB configuration is used in radio transmitters and receivers, RF amplifiers, impedance-matching circuits, oscillators, and wideband amplifiers**,** where a low-resistance signal source needs to drive a high-resistance load efficiently. Since the collector current closely follows the emitter current (current gain α is close to 1), it is also useful in current amplification and signal conditioning circuits**.** Due to the absence of phase reversal and reduced Miller effect, CB configuration performs well in communication and instrumentation applications, though it is rarely used in low-frequency audio amplifiers.

VIVA QUESTIONS:

1. What is Common Base (CB) configuration?
2. Why is it called common base configuration?
3. Which terminal is common in CB configuration?
4. Which terminal acts as input in CB configuration?
5. Which terminal acts as output in CB configuration?
6. What type of biasing is used in CB configuration?
7. Which junction is forward biased in CB configuration?
8. Which junction is reverse biased in CB configuration?
9. What are the input characteristics of CB configuration?
10. What are the output characteristics of CB configuration?
11. What are the transfer characteristics of CB configuration?
12. What is current gain (α) in CB configuration?
13. What is the typical value of α?
14. Why is current gain less than 1 in CB configuration?
15. What is the relationship between α and β?
16. What is the input resistance of CB configuration?
17. What is the output resistance of CB configuration?
18. What is the voltage gain of CB configuration?
19. What is the power gain of CB configuration?
20. What is the phase relationship between input and output signals?
21. What happens to collector current when emitter current increases?
22. Why is input impedance low in CB configuration?
23. Why is output impedance high in CB configuration?
24. Why is CB configuration suitable for high frequency applications?
25. What is the difference between CB and CE configuration?
26. What are the advantages of CB configuration?
27. What are the disadvantages of CB configuration?

28. Where is CB configuration used?
29. Which transistor parameter is maximum in CB configuration?
30. Draw and explain the circuit diagram of CB configuration.

Software-Based Simulation Experiments

Experiment No. 7

Simulate a Zener diode-based voltage regulator to study voltage stabilization against varying supply voltages.

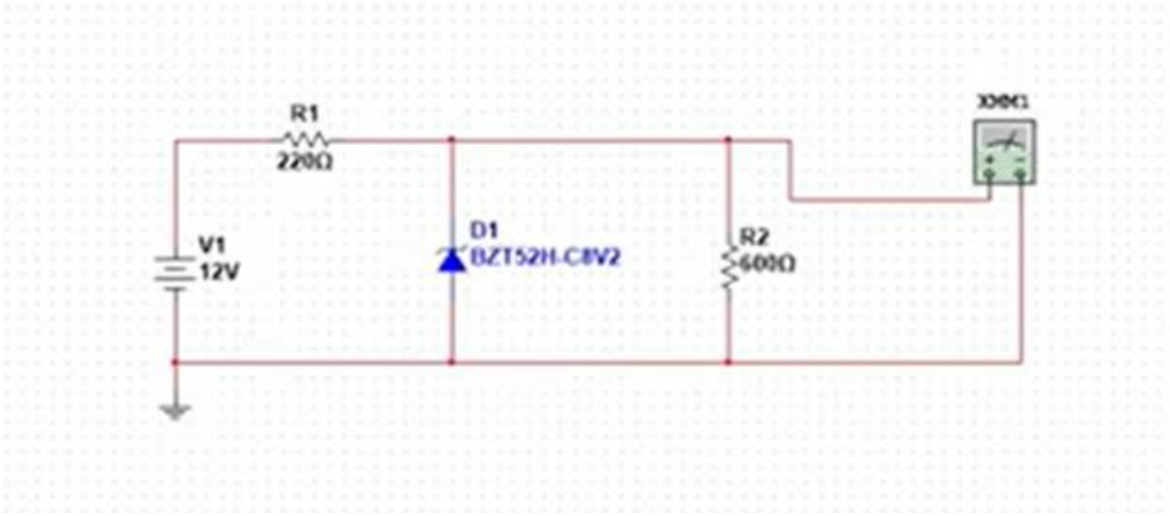
AIM:

To simulate a Zener diode voltage regulator and study the voltage stabilization against varying supply voltages and load resistances.

APPARATUS / COMPONENTS (IN MULTISIM):

1. DC voltage source
2. Series resistor
3. Zener diode
4. Load resistor
5. Multimeter / Voltage probe
6. Multisim software

CIRCUIT DIAGRAM:



PROCEDURE:

Voltage Stabilization with Varying Input Voltage

1. Open Multisim and place the components as shown in the circuit diagram.
2. Set the **Zener diode breakdown voltage** (V_z) according to your specification (e.g., 5.6 V).
3. Set **Rs = 470 Ω** and **R_L = 1 kΩ**.
4. Connect the **DC voltage source Vin** starting slightly above V_z (e.g., 6 V).
5. Simulate the circuit and **measure Vout** across the load resistor.
6. Gradually increase V_{in} (e.g., 6 V → 12 V) and record V_{out} for each value.
7. Observe and note how V_{out} remains nearly constant, demonstrating voltage regulation.

Voltage Stabilization with Varying Load Resistance

1. Keep V_{in} constant (e.g., 12 V).
2. Vary **R_L** from 500 Ω to 5 kΩ.
3. Measure and record **V_{out}** for each R_L.
4. Observe that V_{out} remains nearly constant until the current through the Zener falls below its minimum regulation current.

OBSERVATION TABLE:

Input Voltage V_{in} (V)	Load Resistance R_L (Ω)	Output Voltage(V)

Result: Thus, voltage regulation is successfully verified using Multisim

Experiment No. 8

Simulate a common emitter amplifier with and without emitter bypass capacitor to analyze the effect on voltage gain and signal amplification.

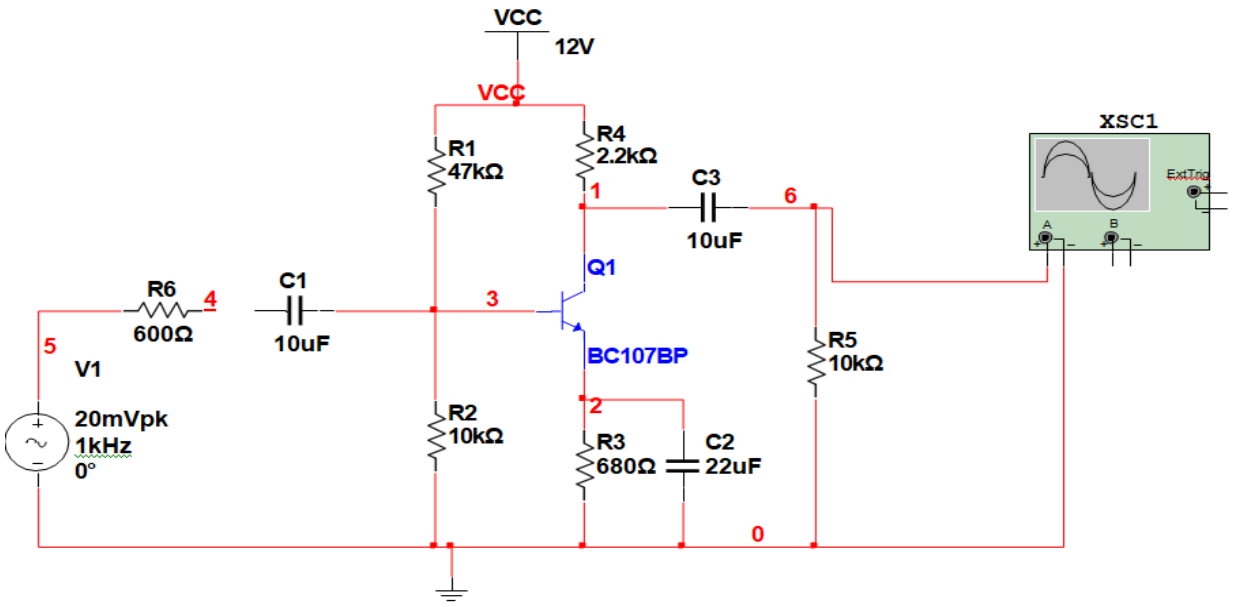
AIM:

To simulate a Common Emitter amplifier using Multisim and study the effect of an emitter bypass capacitor on voltage gain and signal amplification.

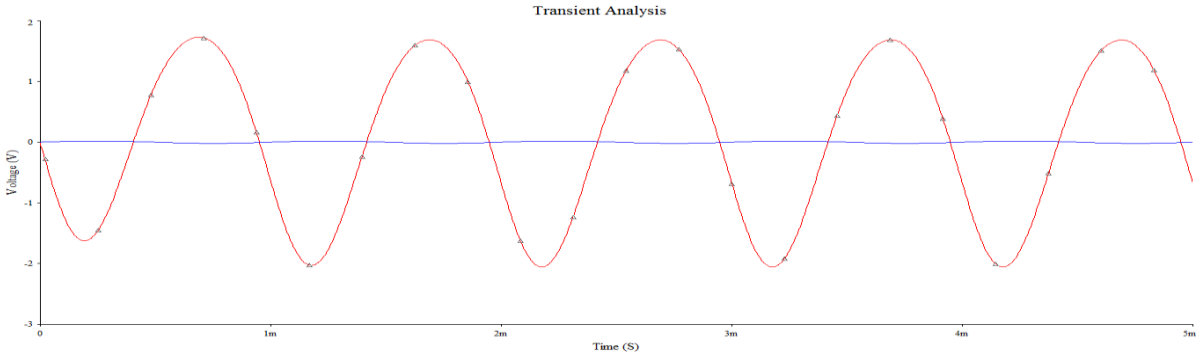
APPARATUS / COMPONENTS (MULTISIM)

1. NPN Transistor
2. DC Power Supply (V_{CC})
3. Signal Generator (AC source)
4. Resistors:
    a. Collector resistor (R_C)
    b. Emitter resistor (R_E)
    c. Base bias resistors (R1, R2)
5. Capacitors:
    a. Input coupling capacitor (C_{in})
    b. Output coupling capacitor (C_{out})
    c. **Emitter bypass capacitor (C_E)**
6. Ground
7. Oscilloscope / Multimeter

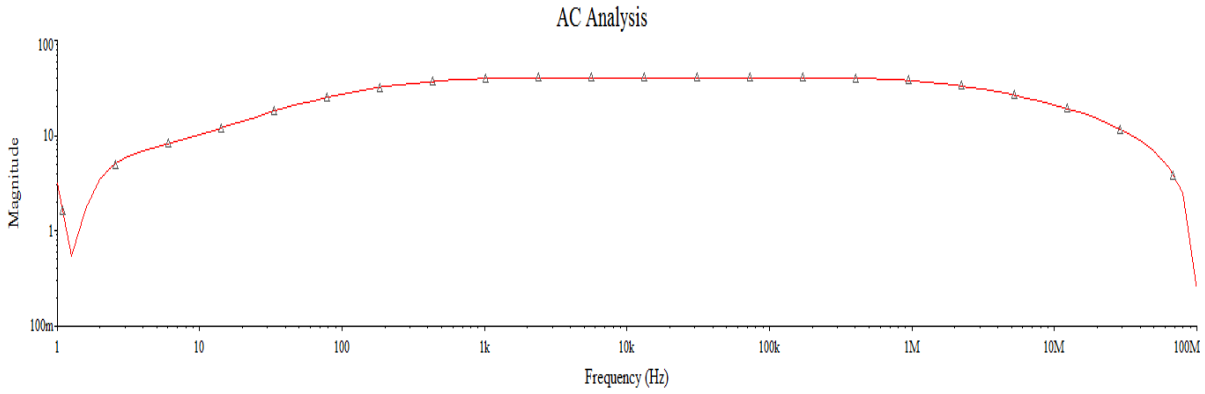
CIRCUIT DIAGRAM:



OUTPUT WAVE FORM:



FREQUENCY RESPONSE:



PROCEDURE:

1. Connect the circuit diagram as shown in the given figure.
2. Apply a sine wave input signal of **1 kHz frequency** and **20 mV (peak) amplitude.**
3. Select **Simulate** and then click on **Run** to start the simulation.
4. Observe the amplified output signal using the **oscilloscope.**
5. To obtain the frequency response, go to **Simulate → Analyses → AC Analysis.**
6. Enter the **start frequency** and **stop frequency** as required.
7. Write the appropriate **expression for voltage gain** and click on **Simulate.**
8. Observe the **magnitude response** and **phase response** of the amplifier.
9. From the magnitude response, **calculate the voltage gain and bandwidth** of the amplifier.

Without Emitter Bypass Capacitor:

1. Remove or disconnect C_E.
2. Run the simulation.
3. Observe input and output waveforms.
4. Measure output amplitude.

OBSERVATION TABLE:

Condition	**Input (mV)**	**Output (V)**	**Voltage Gain $A_v=V_{out}/V_{in}$**
Without C_E			
With C_E			

RESULT:

The Common Emitter amplifier shows higher voltage gain when an emitter bypass capacitor is used.

Without the bypass capacitor, gain is reduced due to emitter degeneration, improving stability but reducing amplification.

PART-B

Experiment No. 1

REALIZATION OF BOOLEAN EXPRESSIONS USING GATES

AIM:

Realization of Boolean Expressions using Gates

APPARATUS:

1. IC 7404
2. IC 7408
3. IC 7432
4. Trainer kit
5. Patch Cords

LOGIC DIAGRAM 1:

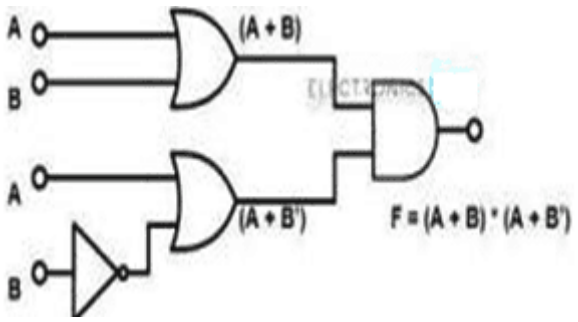


Figure 1.1 Logic Diagram 1

LOGIC DIAGRAM 2

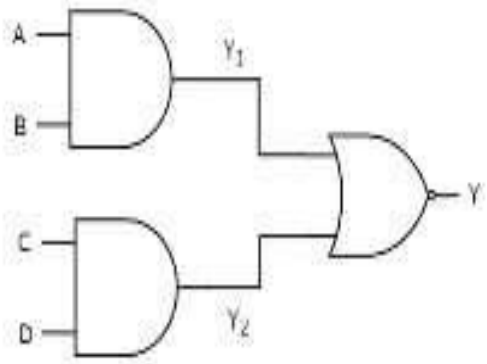
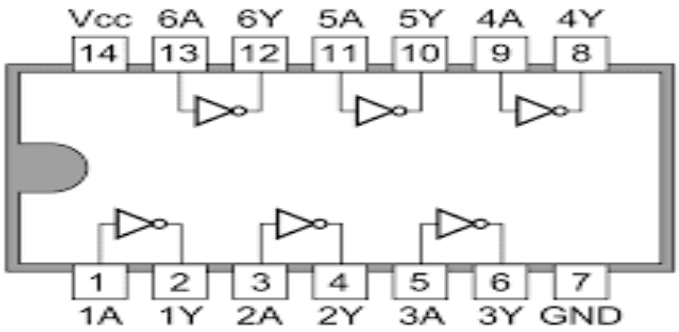


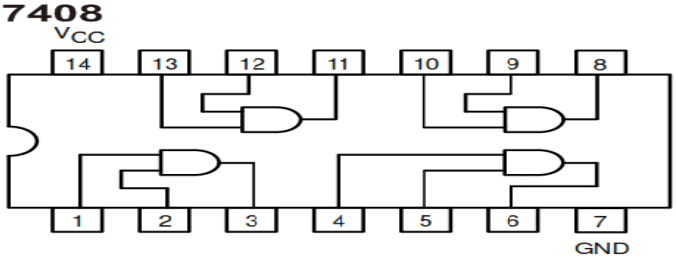
Figure 1.2 Logic Diagram 2

IC PIN DIAGRAMS:

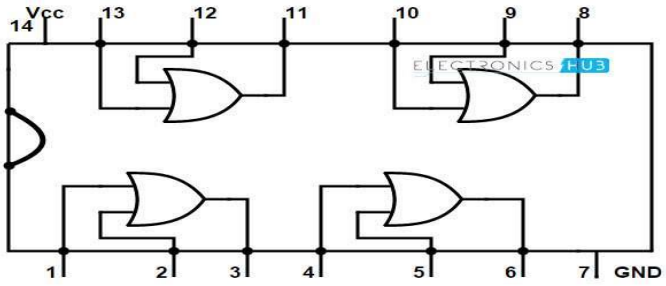
7404 Hex Inverters



7408



7432

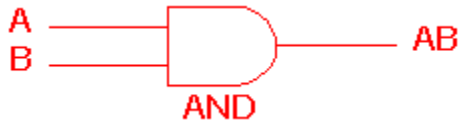


THEORY:

Logic gates

Digital systems are said to be constructed by using logic gates. These gates are the AND, OR, NOT, NAND, NOR, EXOR and EXNOR gates. The basic operations are described below with the aid of truth tables.

AND gate



2 Input AND gate		
A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

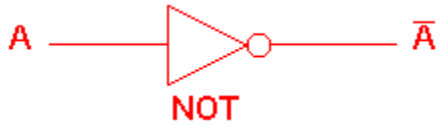
The AND gate is an electronic circuit that gives a **high** output (1) only if **all** its inputs are high. A dot (.) is used to show the AND operation i.e. A.B. Bear in mind that this dot is sometimes omitted i.e. AB

OR gate

2 Input OR gate		
A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

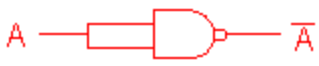
The OR gate is an electronic circuit that gives a high output (1) if **one or more** of its inputs are high. A plus (+) is used to show the OR operation.

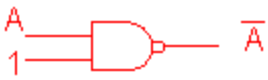
NOT gate



NOT gate	
A	$\overline{A}$
0	1
1	0

The NOT gate is an electronic circuit that produces an inverted version of the input at its output. It is also known as an *inverter*. If the input variable is A, the inverted output is known as NOT A. This is also shown as A', or A with a bar over the top, as shown at the outputs. The diagrams below show two ways that the NAND logic gate can be configured to produce a NOT gate. It can also be done using NOR logic gates in the same way.





NAND gate

2 Input NAND gate		
A	B	$\overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

This is a NOT-AND gate which is equal to an AND gate followed by a NOT gate. The outputs of all NAND gates are high if **any** of the inputs are low. The symbol is an AND gate with a small circle on the output. The small circle represents inversion.

NOR gate

2 Input NOR gate		
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

This is a NOT-OR gate which is equal to an OR gate followed by a NOT gate. The outputs of all NOR gates are low if **any** of the inputs are high.

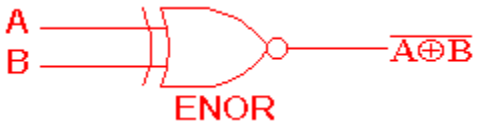
The symbol is an OR gate with a small circle on the output. The small circle represents inversion.

EXOR gate

2 Input EXOR gate		
A	B	A⊕B
0	0	0
0	1	1
1	0	1
1	1	0

The '**Exclusive-OR**' gate is a circuit which will give a high output if **either, but not both**, of its two inputs are high. An encircled plus sign (⊕) is used to show the EOR operation.

EXNOR gate



2 Input EXNOR gate		
A	B	$\overline{A \oplus B}$
0	0	1
0	1	0
1	0	0
1	1	1

The '**Exclusive-NOR**' gate circuit does the opposite to the EOR gate. It will give a low output if **either, but not both**, of its two inputs are high. The symbol is an EXOR gate with a small circle on the output. The small circle represents inversion.

The NAND and NOR gates are called *universal functions* since with either one the AND and OR functions and NOT can be generated.

Note:

A function in *sum of products* form can be implemented using NAND gates by replacing all AND and OR gates by NAND gates.

A function in *product of sums* form can be implemented using NOR gates by replacing all AND and OR gates by NOR gates

Table 1: Logic gate symbols

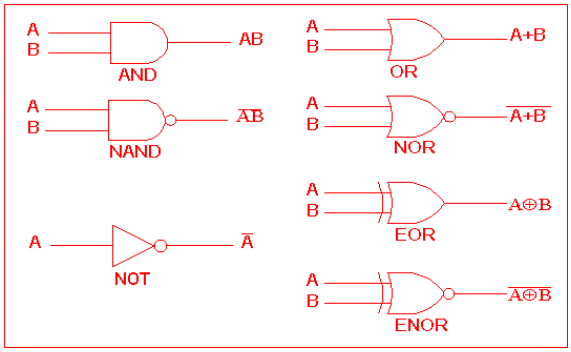


Table 2 is a summary truth table of the input/output combinations for the NOT gate together with all possible input/output combinations for the other gate functions. Also note that a truth table with 'n' inputs has 2^n rows. You can compare the outputs of different gates.

Table 2: Logic gates representation using the Truth table

NOT gate	
A	$\overline{A}$
0	1
1	0

INPUTS		OUTPUTS					
A	B	AND	NAND	OR	NOR	EXOR	EXNOR
0	0	0	1	0	1	0	1
0	1	0	1	1	0	1	0
1	0	0	1	1	0	1	0
1	1	1	0	1	0	0	1

TRUTH TABLE:

Logic diagram 1:

A	B	A+B	B’	A+B’	F= (A+B)*(A+B’)

Logic diagram 2:

A	**B**	**Y1=A*B**	**C**	**D**	**Y2=C*D**	**(A*B)+(C*D)**	**Y= ((A*B)+(C*D))’**

PROCEDURE:

1. Make the connections as per the circuit diagram
2. Switch on the power supply
3. Verify the truth table

PRECAUTIONS:

1. The power supply pins must be checked whether power is available at those pins using test probes.
2. No loose connections should be there and care must be taken to avoid shorting of pins.

REAL TIME APPLICATIONS:

Realization of Boolean expressions using logic gates is used to design digital circuits like adders and multiplexers.

It forms the basic operation of computers, calculators, and microprocessors.

Applications include control systems, communication devices, and digital electronics hardware.

RESULT:

Realization of Boolean Expressions using Gates AND ,OR and NOT gates NOR gates have been verified.

VIVA QUESTIONS:

1. The boolean expression of an OR gate is _____?
2. A _____ gate gives the output as 1 only if all the inputs signals are?
3. Which of the gate will give a 0 when both of its inputs are 1?
4. The gate which is called an inverter is called _____?
5. The expression of an EXOR gate is _____?
6. When logic gates are connected to form a gating/logic network it is called as a _____ logic circuit.
7. The universal gate that can be used to implement any Boolean expression is _____?
8. Electronic circuits that operate on one or more input signals to produce standard output _____?
9. What are the universal gates?
10. A _____ is a circuit with only one output but can have multiple inputs?
11. The Output is LOW if any one of the inputs is HIGH in case of a _____ gate?
12. How many AND gates are required to realize the following expression Y=AB+BC?
13. Number of outputs in a half adder _____
14. The expression of a NAND gate is_____?
15. The _____ gate is an OR gate followed by a NOT gate?
16. Brain of computer is _____?
17. What does MBR stand for?
18. In the instruction ADD A, B, the answer gets stored in _____?
19. What does PC stand for?
20. Which of the following holds the last instruction fetched?

21. The portion of the processor which contains the hardware required to fetch the operations is _____?
22. Causing the CPU to step through a series of micro operations is called _____?
23. The functions of execution and sequencing are performed by using _____?
24. What does D in the D-flip flop stand for?
25. The length of a register is called _____?
26. Opcode indicates the operations to be performed?
27. CPU has built-in ability to execute a particular set of machine instructions, called as _____?
28. Write two characterstics of combinational circuits?
29. Explain what is excitation table?
30. Explain what is Boolean Algebra?

Experiment No. 2

DESIGN AND REALIZATION LOGIC GATES USING UNIVERSAL GATES

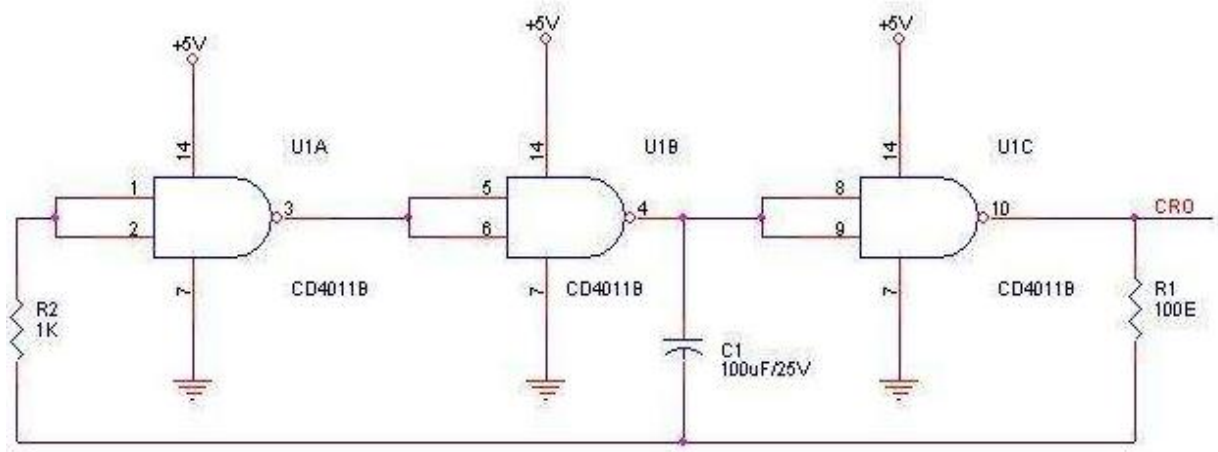
AIM:

Generation of clock using NAND / NOR gates

APPARATUS:

1. Patch Cords
2. IC CD 4011
3. 1k Resistance
4. 100E Resistance
5. 100uF/25V Electrolytic Capacitor
6. Bread Board

CIRCUIT DIAGRAM:



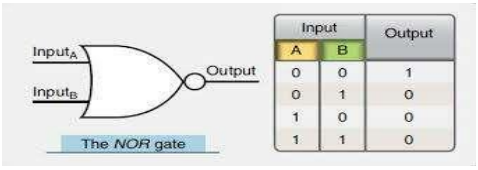
THEORY:

NAND Gate: The NAND gate represents the complement of the AND operation. Its name is an abbreviation of NOT AND. The graphic symbol for the NAND gate consists of an AND symbol with a bubble on the output, denoting that a complement operation is performed on

the output of the AND gate. The truth table and the graphic symbol of NAND gate is shown in the figure. The truth table clearly shows that the NAND operation is the complement of the AND.

Inputs		output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

NOR Gate: The NOR gate represents the complement of the OR operation. Its name is an abbreviation of NOT OR. The graphic symbol for the NOR gate consists of an OR symbol with a bubble on the output, denoting that a complement operation is performed on the output of the OR gate. The truth table and the graphic symbol of NOR gate is shown in the figure. The truth table clearly shows that the NOR operation is the complement of the OR.



Universal Gates: A universal gate is a gate which can implement any Boolean function without need to use any other gate type. The NAND and NOR gates are universal gates. In practice, this is advantageous since NAND and NOR gates are economical and easier to fabricate and are the basic gates used in all IC digital logic families. In fact, an AND gate is typically implemented as a NAND gate followed by an inverter not the other way around!! Likewise, an OR gate is typically implemented as a NOR gate followed by an inverter

PROCEDURE:

1. Make the connection as per the above connection diagram.
2. Switch On the power supply.
3. Observed the output on the CRO.
4. BY changing the value of R1, R2 and C1 to change the Clock Output.

PRECAUTIONS:

1. The power supply pins must be checked whether power is available at those pins using test probes.
2. No loose connections should be there and care must be taken to avoid shorting of pins.

RESULT: Clock signal is generated successfully by using nand/nor gate.

VIVA QUESTIONS:

1. What are the universal gates? Why they are called so?
2. Realize the EX – OR gates using minimum number of NAND gates.
3. Give the truth table for EX-NOR and realize using NAND gates?
4. What are the logic low and High levels of TTL IC's and CMOS IC's?
5. Compare TTL logic family with CMOS family?
6 .Which logic family is fastest and which has low power dissipation?
7. What are the different methods to obtain minimal expression?
8.What is a Min term and Max term
9. State the difference between SOP and POS.
10. What is K-map? Why is it used?
11.What do you mean by Logic Gates?
12.What are the applications of Logic Gates?
13.What is Truth Table?
14. Why we use basic logic gates?
15.Write down the truth table of all logic gates?
16.What do you mean by universal gate?
17.Write truth table for 2 input NOR,NAND gate?
18. Implement all logic gate by using universal gate?
19.Why is they called universal Gates?
20. Give the name of universal gate?
21. Draw the circuit diagram of Half adder circuit?
22.Draw the circuit diagram of full adder circuit?
23 Draw the full adder circuit by using Half Adder circuit and minimum no. of logicgate?
24.Write Boolean function for half adder?
25. Write Boolean function for Full adder?261.Design the half Adder and Full adder using NAND-NAND Logic.
26.Pseudo Random Sequence Generator also known as what?

27.Ring counter belong to which type of counter?

28.What are the types of ring counter?

29. What is the difference between Johnson Ring Counter and synchronous ring counter?

30.What is meant by pseudorandom number generator?

Experiment No. 3

Generation of clock using NAND/NOR gates

AIM:

To design 450KHZ clock using nand/nor gates.

APPARATUS: Clock generator trainer kit, Patch cords

THEORY:

Pulse generator using NAND gate:

This simple pulse generator using NAND gate is very useful and can be used as clock generator for other circuits. The circuit's main element is a 2 input NAND gate connected as NOT gate

A NAND gate can be used as an oscillator by providing feedback through an RC network. The resistor and capacitor introduce a time delay, which causes the output to continuously switch between HIGH and LOW, generating a clock pulse.

Frequency of Oscillation

The clock frequency mainly depends on the **RC time constant**.

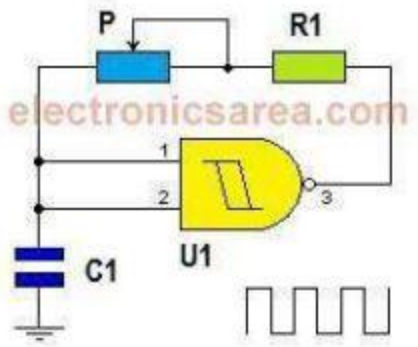
$$f \approx 1/1.4RC$$

Where:

- R = Resistance
- C = Capacitance

Clock Generation Using NOR Gate:

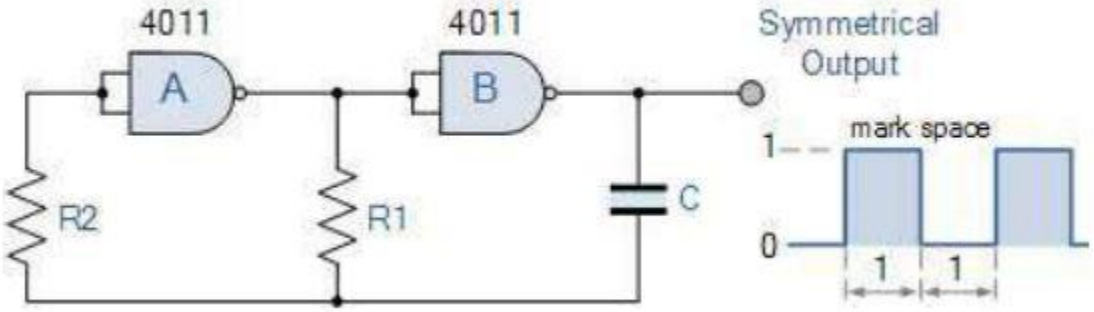
Similar to NAND, a **NOR gate can also generate clock pulses** using an **RC feedback network**. The RC network provides the delay required for oscillation.



SQUARE WAVE GENERATOR USING NAND GATE:

Square waves are extensively used in many digital circuits. Many combinational logic circuits require this wave to operate. Here are few methods you can generate simple square wave using NAND, Inverter and Schmitt Trigger gates. These kind of square wave generator fit perfectly for simple oscillator applications with minimum effort required to build.

CIRCUIT DIAGRAM:



Procedure:

1.Connect the circuit as per the circuit diagram.

2.Apply the different values of resistors and capacitors and the observe the frequency .

3. Repeat the process for different combinations of resistors and capacitors.

4. Compare the theoretical and practical values of frequencies

PRECAUTIONS:

1. The power supply pins must be checked whether power is available at those pins using test probes.
2. No loose connections should be there and care must be taken to avoid shorting of pins.

Result:

Thus, a clock signal was successfully generated using NAND/NOR gates with the help of an RC feedback network.

VIVA QUESTIONS:

1. What is a **clock signal**?
2. Why is a **clock signal required in digital circuits**?
3. What is meant by a **clock pulse**?
4. What type of waveform is a **clock signal**?
5. What is meant by **oscillator**?
6. What is the purpose of **clock generation circuits**?
7. What is a **NAND gate**?
8. What is a **NOR gate**?
9. Why are **NAND and NOR gates called universal gates**?
10. How can a **NAND gate be used to generate clock pulses**?
11. How can a **NOR gate be used as an oscillator**?
12. What is the role of **feedback** in clock generation circuits?
13. What components are required to generate a clock using NAND/NOR gates?
14. What is the function of a **resistor in the RC network**?
15. What is the function of a **capacitor in the circuit**?
16. What is meant by **RC time constant**?
17. How does the **capacitor charging and discharging** create oscillation?
18. What happens when the **capacitor is fully charged**?
19. What happens when the **capacitor discharges**?
20. What type of signal is obtained at the **output**?
21. What determines the **frequency of the clock signal**?
22. Write the **frequency formula of RC oscillator**.
23. Where are **clock pulses used**?
24. Why are clock signals important in **sequential circuits**?
25. Name some circuits that require **clock signals**.
26. Can clock signals be generated using **other gates**?
27. What is the difference between **clock signal and pulse signal**?

28. What happens if the **RC values are changed**?
29. Why is **time delay important** in oscillator circuits?
30. What are the **applications of NAND/NOR gate clock generators**?

Experiment No. 4

DESIGN A 4 – BIT ADDER / SUBTRACTOR

AIM:

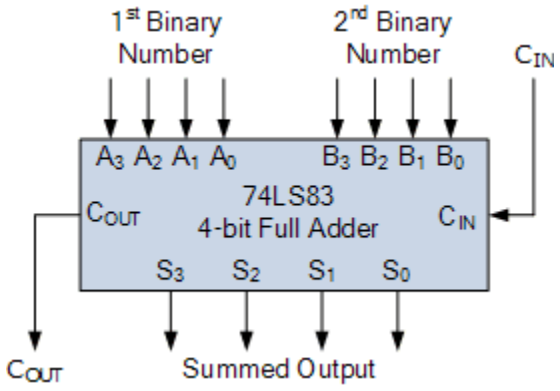
Design a 4 – bit Adder / Subtractor

APPARATUS:

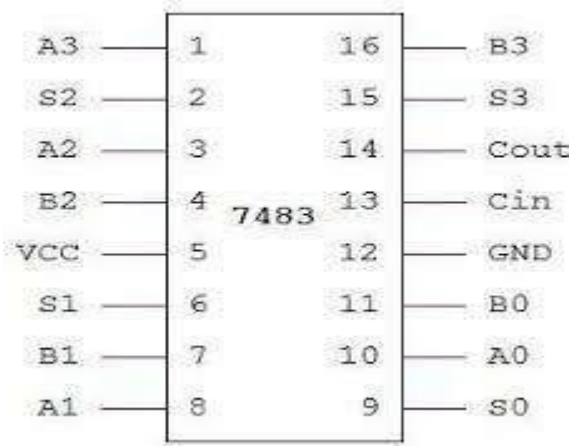
1. IC 7408
2. IC 7432
3. IC 7486
4. Bread Board
5. Connecting wires

BLOCK DIAGRAM:

4-BIT ADDER USING 74LS83:



IC 74LS83 PIN DIAGRAM:



TRUTH TABLE:

	A				B				Sum				Carry
Cin	A3	A2	A1	A0	B3	B2	B1	B0	S3	S2	S1	S0	Cout
0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	1	0	0	1	0	0
0	0	0	1	0	0	0	1	0	0	1	0	0	0
0	0	0	1	1	0	0	1	1	0	1	1	0	0
0	0	1	0	0	0	1	0	0	1	0	0	0	0
0	0	1	0	1	0	1	0	1	1	0	1	0	0
0	0	1	1	0	0	1	1	0	1	1	0	0	0
0	0	1	1	1	0	1	1	1	1	1	1	0	0
0	1	0	0	0	1	0	0	0	0	0	0	0	1
0	1	0	0	1	1	0	0	1	0	0	1	0	1
0	1	0	1	0	1	0	1	0	0	1	0	0	1
0	1	0	1	1	1	0	1	1	0	1	1	0	1
0	1	1	0	0	1	1	0	0	1	0	0	0	1
0	1	1	0	1	1	1	0	1	1	0	1	0	1
0	1	1	1	0	1	1	1	0	1	1	0	0	1
0	1	1	1	1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

THEORY:

FOUR-BIT BINARY PARALLEL ADDER:

In the preceding section, we discussed how two binary bits can be added and the addition of two binary bits with a carry. In practical situations it is required to add two data each containing more than one bit. Two binary numbers each of *n* bits can be added by means of a full adder circuit. Consider the example that two 4-bit binary numbers $B_4B_3B_2B_1$ and $A_4A_3A_2A_1$ are to be added with a carry input C_1. This can be done by cascading four full adder circuits as shown in Figure 5.48. The least significant bits A_1, B_1, and C_1 are added to the produce sum output S_1 and carry output C_2. Carry output C_2 is then added to the next significant bits A_2 and B_2 producing sum output S_2 and carry output C_3. C_3 is then added to A_3 and B_3 and so on. Thus finally producing the four-bit sum output $S_4S_3S_2S_1$ and final carry output Cout. Such type of four-bit binary adder is commercially available in an IC package. For the addition of two *n* bits of data, *n* numbers of full adders can be cascaded as

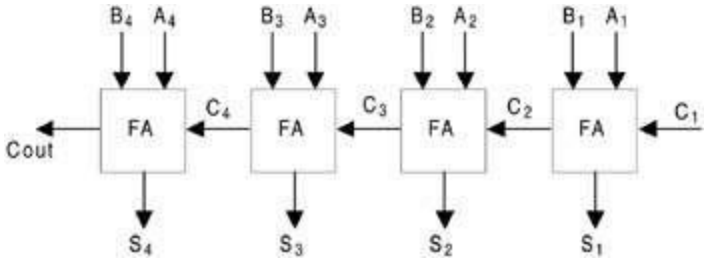


Figure 4.1 4-Bit Full Adder

PROCEDURE:

1. Connections are made as per the circuit diagram
2. Switch on the supply

3. Apply the input values
4. Verify the truth table for different input values

PRECAUTIONS:

1. Connection should be tight.
2. O/P should be finding sequentially.
3. IC's should be handled carefully.

REAL TIME APPLICATIONS:

A 4-bit adder/subtractor is used in arithmetic logic units (ALUs) of microprocessors to perform addition and subtraction.

It is applied in calculators and digital computing systems for basic arithmetic operations.

It is also used in embedded systems and control units for data processing.

RESULT: The operation of 4 Bit Adder has been verified.

VIVA QUESTIONS:

1. How many basic binary subtraction operations are possible?
2. What are the two types of basic adder circuits?
3. A binary parallel adder produces arithmetic sum in what?
4. Total number of inputs in a half adder is
5. Controlled inverter is also known as
6. A logic circuit that provides a HIGH output for both inputs HIGH or both inputs LOW is
7. What is the major difference between half-adders and full-adders?
8. How many basic binary subtraction operations are possible?
9. What are the two types of basic adder circuits?
10. When performing subtraction by addition in the 2's-complement system:
11. What is a 4 bit adder?
12. What is a subtractor?
13. Describe the function of a full adder?
14. Design a full adder using two half adders?
15. What is the difference between half adder and a full adder?
16. Write the applications of adders and subtractors?
17. Draw the logic diagram of adder?
18. Draw the logic diagram of a subtractor?
19. What is the use of adder in digital circuits?
20. Is it possible to construct a circuit to perform both addition and subtraction at the same time?
21. How are adders used in processors? Explain.
22. Carry is obtained in which operation?
23. What are the limitations of half adders?
24. How many logic gates are required for designing a full adder and what are they?
25. How many number of inputs does a half adder and a full adder have?
26. For upto how many bits can a half subtractor perform subtraction?
27. What are the bits which undergo subtraction operation in half subtractors?
28. How many outputs are required for a adder and a subtractor?
29. Describe minuend?
30. Describe subtrahend?

Experiment No. 5

Design and realization a 4 – bit gray to Binary and Binary to Gray Converter

Aim: To Design and realization a 4 bit gray to Binary and Binary to Gray Converter

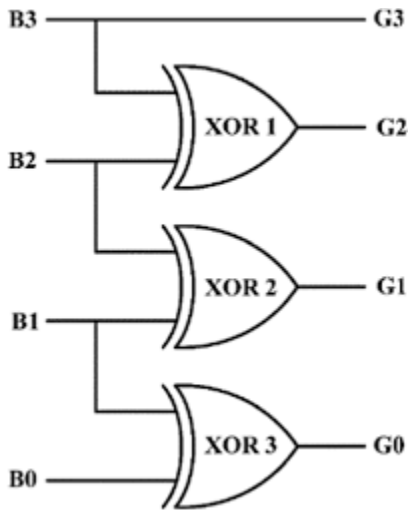
Apparatus: Binary to gray logic trainer kit, Patch cords

Theory:

Binary to Gray Code Converter

The logical circuit which converts binary code to equivalent gray code is known as binary to gray code converter. The gray code is a non weighted code. The successive gray code differs in one bit position only that means it is a unit distance code. It is also referred as cyclic code. It is not suitable for arithmetic operations. It is the most popular of the unit distance codes. It is also a reflective code. An n-bit Gray code can be obtained by reflecting an n-1 bit code about an axis after 2 n-1 rows, and putting the MSB of 0 above the axis and the MSB of 1 below the axis. Reflection of Gray codes is shown below. The 4 bits binary to gray code conversion table is given below

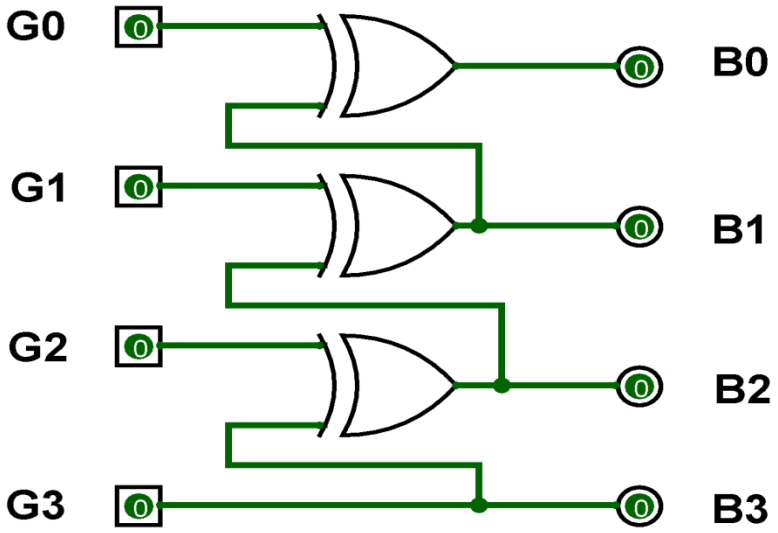
The 4 bits binary to gray code conversion table & Circuit Diagram is given below



Natural-binary code				Gray code			
B3	B2	B1	B0	G3	G2	G1	G0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

The 4 bits gray code to binary conversion table & Circuit Diagram is given below

4 bit Gray Code	4 bit Binary Code
A B C D	B_4 B_3 B_2 B_1
0 0 0 0	0 0 0 0
0 0 0 1	0 0 0 1
0 0 1 1	0 0 1 0
0 0 1 0	0 0 1 1
0 1 1 0	0 1 0 0
0 1 1 1	0 1 0 1
0 1 0 1	0 1 1 0
0 1 0 0	0 1 1 1
1 1 0 0	1 0 0 0
1 1 0 1	1 0 0 1
1 1 1 1	1 0 1 0
1 1 1 0	1 0 1 1
1 0 1 0	1 1 0 0
1 0 1 1	1 1 0 1
1 0 0 1	1 1 1 0
1 0 0 0	1 1 1 1



Procedure:

1. Connect the circuit as per the circuit diagram.
2. Connect the inputs to the switch and outputs to the logic indicators.
3. Apply the different combinations of inputs and observe the outputs.

PRECAUTIONS:

1. The power supply pins must be checked whether power is available at those pins using test probes.
2. No loose connections should be there and care must be taken to avoid shorting of pins.

Real-Time Applications of Binary to Gray (BTOG) and Gray to Binary (GTOB):

1. **Rotary Position Encoders**

   Gray code is widely used in **rotary encoders** to detect the position of rotating shafts in motors and robotic arms. Binary values are converted to Gray code (BTOG) to reduce errors during position detection, and then converted back to binary (GTOB) for digital processing.

2. **Analog to Digital Converters (ADCs)**
   In some ADC designs, **Gray code is used to minimize switching errors** between adjacent values. The Gray code output is later converted back to binary for computation.
3. **Digital Communication Systems**
   Gray code is used in **modulation techniques** (like QAM) to reduce bit errors during signal transmission. Conversion between binary and Gray code helps improve reliability.
4. **Karnaugh Map (K-Map) Arrangement**
   Gray code is used in arranging **K-maps** so that only one variable changes between adjacent cells, simplifying Boolean function minimization.
5. **Error Reduction in Digital Systems**
   Gray code ensures that **only one bit changes between successive numbers**, reducing errors in high-speed digital circuits.
6. **Robotics and Automation Systems**
   Used in **robot joint position sensing** and automated machines where precise movement tracking is required.
7. **Counters and Digital Instruments**
   Gray code counters are used in **digital measurement systems** to avoid transition errors.
8. **Memory Addressing and Data Conversion**
   Some systems convert **binary addresses to Gray code** to reduce switching noise and then convert back to binary for processing.

RESULT:

Thus, the Binary to Gray code conversion was successfully implemented**,** and the obtained Gray code outputs matched the expected values for the given binary inputs**.**

Thus, the Gray to Binary code conversion was successfully implemented**,** and the obtained binary outputs matched the expected values for the given Gray code inputs**.**

VIVA QUESTIONS:

1. What is a Binary code?
2. What is Gray code?
3. Why is Gray code called reflected binary code?
4. What is the main advantage of Gray code?
5. Where is Gray code commonly used?
6. What is meant by code conversion in digital electronics?
7. What is Binary to Gray code conversion (BTOG)?
8. What is the rule for converting Binary to Gray code?
9. How is the first Gray bit obtained from binary?
10. How are the remaining Gray bits calculated?
11. Which logic gate is used for Binary to Gray conversion?
12. Write the logic expression for Binary to Gray conversion.
13. What is Gray to Binary conversion (GTOB)?
14. What is the rule for converting Gray code to Binary?
15. How is the first binary bit obtained from Gray code?
16. How are the remaining binary bits calculated?
17. Which logic gate is mainly used in Gray to Binary conversion?
18. Why is XOR gate important in code conversion circuits?
19. How many bits change between two successive Gray codes?
20. Why is Gray code preferred in digital systems?
21. What is the difference between Binary code and Gray code?
22. What type of errors can Gray code reduce?
23. Where is Gray code used in encoders?
24. Why is Gray code used in position encoders?
25. What are the applications of code converters?
26. Can combinational circuits be used for code conversion?

27. Draw the logic circuit for Binary to Gray converter.
28. Draw the logic circuit for Gray to Binary converter.
29. What are the advantages of Gray code over binary code?
30. What will happen if more than one bit changes at a time in binary code?

Experiment No. 6

DESIGN AND REALIZATION OF AN 8 BIT PARALLEL LOAD AND SERIAL OUT SHIFT REGISTER USING FLIP-FLOPS

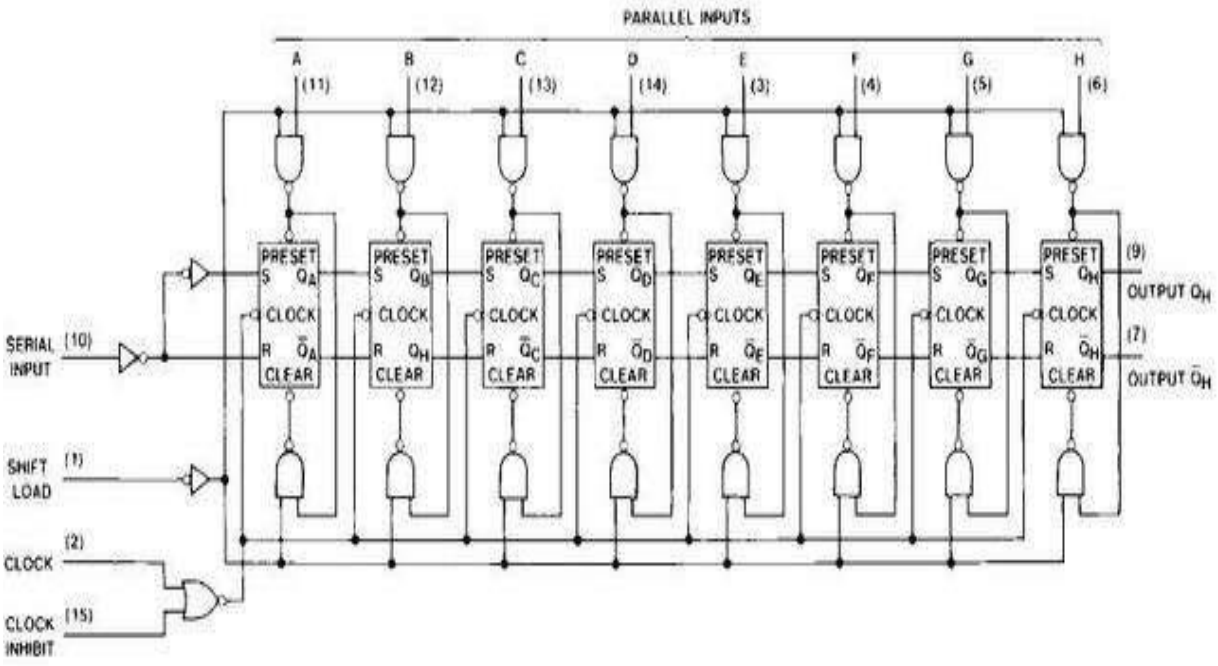
AIM:

Design and realization of an 8 bit parallel load and serial out shift register using flip-flops.

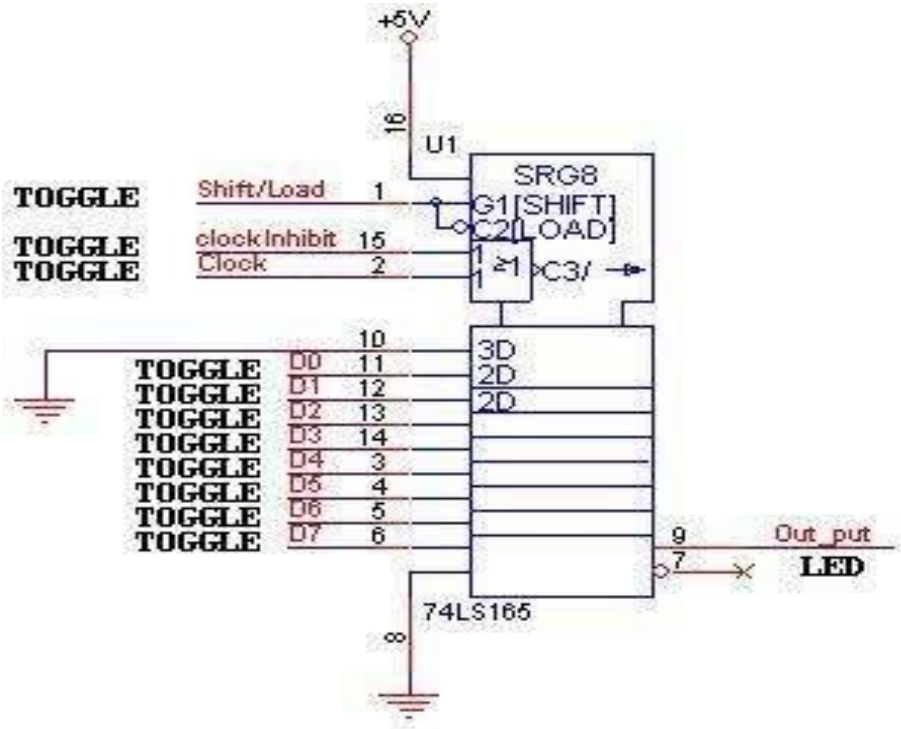
APPARATUS:

1. Patch Cords
2. IC 74LS165
3. Trainer kit

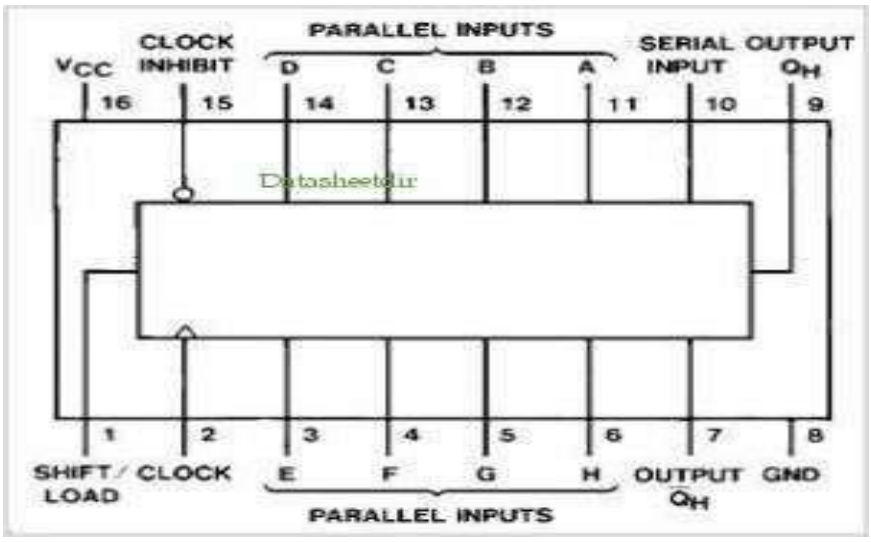
BLOCK DIAGRAM:



CIRCUIT DIAGRAM:



PIN DIAGRAM OF IC 74LS165:



TRUTH TABLE:

CP	D_{IN}	Q_A	Q_B	Q_C	Q_D
Initial	1	0	0	0	0
1st	1	1	0	0	0
2nd	1	1	1	0	0
3rd	1	1	1	1	0
4th	1	1	1	1	1

Shift from left to right

THEORY:

The Shift Register is another type of sequential logic circuit that can be used for the storage or the transfer of binary data

This sequential device loads the data present on its inputs and then moves or "shifts" it to its output once every clock cycle, hence the name **Shift Register**.

A *shift register* basically consists of several single bit "D-Type Data Latches", one for each data bit, either a logic "0" or a "1", connected together in a serial type daisy-chain arrangement so that the output from one data latch becomes the input of the next latch and so on.

Data bits may be fed in or out of a shift register serially, that is one after the other from either the left or the right direction, or all together at the same time in a parallel configuration.

The number of individual data latches required to make up a single **Shift Register** device is usually determined by the number of bits to be stored with the most common being 8-bits (one byte) wide constructed from eight individual data latches.

Shift Registers are used for data storage or for the movement of data and are therefore commonly used inside calculators or computers to store data such as two binary numbers before they are added together, or to convert the data from either a serial to parallel or parallel to serial format. The individual data latches that make up a single shift register are all driven by a common clock (Clk) signal making them synchronous devices.

Shift register IC's are generally provided with a *clear* or *reset* connection so that they can be "SET" or "RESET" as required. Generally, shift registers operate in one of four different modes with the basic movement of data through a shift register being:

- Serial-in to Parallel-out (SIPO) - the register is loaded with serial data, one bit at a time, with the stored data being available at the output in parallel form.
- Serial-in to Serial-out (SISO) - the data is shifted serially "IN" and "OUT" of the register, one bit at a time in either a left or right direction under clock control.
- Parallel-in to Serial-out (PISO) - the parallel data is loaded into the register simultaneously and is shifted out of the register serially one bit at a time under clock control.
- Parallel-in to Parallel-out (PIPO) - the parallel data is loaded simultaneously into the register, and transferred together to their respective outputs by the same clock pulse.

Parallel-in to Serial-out (PISO) Shift Register

The Parallel-in to Serial-out shift register acts in the opposite way to the serial-in to parallel-out one above. The data is loaded into the register in a parallel format in which all the data bits enter their inputs simultaneously, to the parallel input pins P_A to P_D of the register. The data is then read out sequentially in the normal shift-right mode from the register at Qrepresenting the data present at P_A to P_D.

This data is outputted one bit at a time on each clock cycle in a serial format. It is important to note that with this type of data register a clock pulse is not required to parallel load the register as it is already present, but four clock pulses are required to unload the data.

PROCEDURE:

1. Make the connection as per the above connection diagram.
2. Switch On the power supply.
3. Set the data by the toggle switch.
4. Set the Clock by the toggle switch.
5. Set the Preset by the toggle switch.
6. Set the Clear by the toggle switch.
7. Observed the output on the LEDs

PRECAUTIONS:

1. Connection should be tight.
2. O/P should be finding sequentially.
3. IC's should be handled carefully.

REAL TIME APPLICATIONS:

An 8-bit parallel load and serial out (PISO) shift register is used to convert parallel data into serial data.

It is widely used in data communication systems to reduce the number of transmission lines. Applications include microprocessor interfacing, data transmission, and digital communication devices.

RESULT: Parallel load and serial out shift register operation is verified by using truth table

VIVA QUESTIONS:

1. Define shift registers?
2. List the different types of shift registers?
3. The full form of SIPO is
4. A shift register that will accept a parallel input or a bidirectional serial load and internal shift features is called as?
5. What is meant by parallel load of a shift register?
6. With a 200 khz clock frequency, eight bits can be serially entered into a shift register in
7. Based on how binary information is entered or shifted out, shift registers are classified into categories.
8. A serial in/parallel out, 4-bit shift register initially contains all 1s. The data nibble 0111 is waiting to enter. After four clock pulses, the register contains
9. A sequence of equally spaced timing pulses may be easily generated by which type of counter circuit
10. To operate correctly, starting a ring shift counter requires
11. Define shift registers
12. List out different types of shift registers.
13. The full form of SIPO is
14. A shift register that will accept a parallel input or a bidirectional serial load and internal shift features is called as?
15. What is meant by parallel load shift registesr?
16. With a 200khz clock frequency eight bits can be entered into a shift register in.
17. Based on how binary information is entered or shifted out,shift registers are classified into categories.
18. A serial in/parallel out 4 bit shift register initially contains all 1’s the data nibble 0111 is waiting to enter.after four clock pulses,the register contains?
19. .a sequence of equally spaced timing pulses may be easily generated by which type of counter circuit?

20. To operate correctly,starting a ring shift counter requires.
21. Explain the difference between *serial* digital data and *parallel* digital data
22. What is the definition of a *register* in the context of digital circuitry? Also, define and compare/contrast what a *shift register* is.
23. Draw the schematic diagram for a five-bit serial-in/serial-out shift register circuit, and be prepared to give a brief explanation of how it functions.
24. Explain how a shift register circuit could be built from D-type flip-flops with the ability to shift data either to the right or to the left, on command.
25. Explain what a *universal* shift register is
26. Describe how we can get parallel data entered into a shift register circuit.
27. A shift register that will accept a parallel input or a bidirectional serial load and internal shift features is called as?
28. How can parallel data be taken out of a shift register simultaneously?
29. What is meant by parallel load of a shift register?
30. The group of bits 11001 is serially shifted (right-most bit first) into a 5-bit parallel output shift register with an initial state 01110. After three clock pulses, the register contains?

Experiment No. 7

DESIGN AND REALIZATION 8X1 MUX USING 2X1 MUX

AIM:

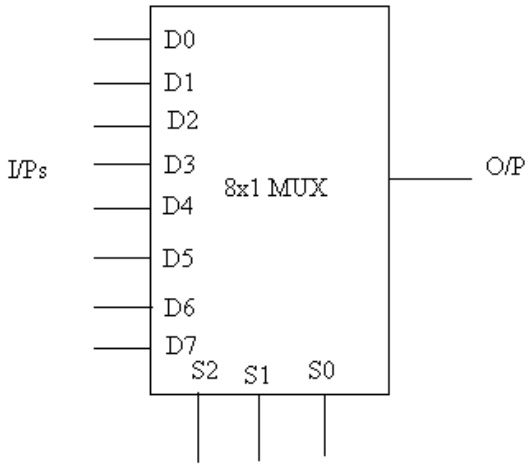
Design and realization of 8x1 MUX using 2x1 MUX

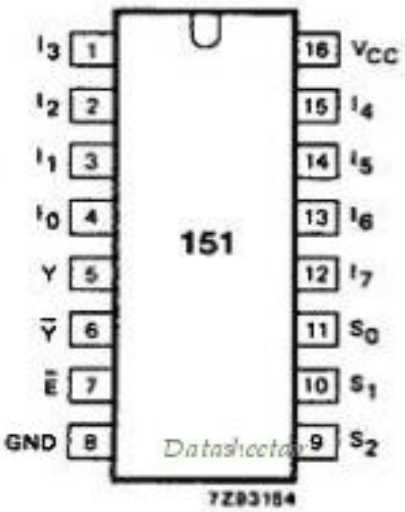
APPARATUS:

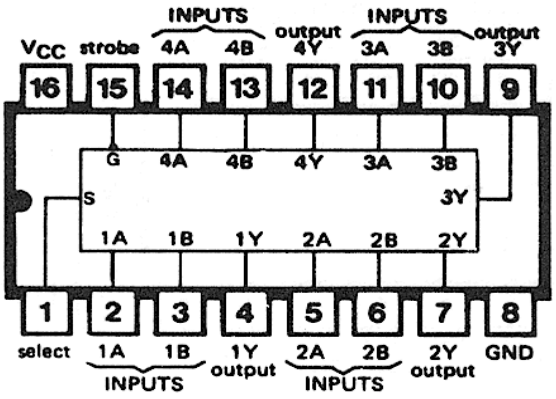
1. IC 74151
2. IC 74157
3. IC 7404
4. Trainer kit
5. Connecting wires
6. Patch Cords

BLOCK DIAGRAM:

IC Pin description of 74HC151







Function table for 8x1 MUX:

Chip Enable(E)	Selection lines S2	S1	S0	Output

THEORY:

8x1 Multiplexer :

In this section, let us implement 8x1 Multiplexer using 4x1 Multiplexers and 2x1 Multiplexer. We know that 4x1 Multiplexer has 4 data inputs, 2 selection lines and one output. Whereas, 8x1 Multiplexer has 8 data inputs, 3 selection lines and one output.

So, we require two 4x1 Multiplexers in first stage in order to get the 8 data inputs. Since, each 4x1 Multiplexer produces one output, we require a 2x1 Multiplexer in second stage by considering the outputs of first stage as inputs and to produce the final output.

Let the 8x1 Multiplexer has eight data inputs I7 to I0, three selection lines s2, s1 & s0 and one output Y. The Truth table of 8x1 Multiplexer is shown below.

We can implement 8x1 Multiplexer using lower order Multiplexers easily by considering the above Truth table. The block diagram of 8x1 Multiplexer is shown in the following figure.

The same selection lines, s1 & s0 are applied to both 4x1 Multiplexers. The data inputs of upper 4x1 Multiplexer are I7 to I4 and the data inputs of lower 4x1 Multiplexer are I3 to I0. Therefore, each 4x1 Multiplexer produces an output based on the values of selection lines, s1 & s0.

The outputs of first stage 4x1 Multiplexers are applied as inputs of 2x1 Multiplexer that is present in second stage. The other selection line, s2 is applied to 2x1 Multiplexer.

- If s2 is zero, then the output of 2x1 Multiplexer will be one of the 4 inputs I3 to I0 based on the values of selection lines s1 & s0.

- If s2 is one, then the output of 2x1 Multiplexer will be one of the 4 inputs I7 to I4 based on the values of selection lines s1 & s0.

Therefore, the overall combination of two 4x1 Multiplexers and one 2x1 Multiplexer performs as one 8x1 Multiplexer.

PROCEDURE:

1. Make the connections as per the circuit diagram
2. Switch on the power supply
3. Verify truth table

PRECAUTIONS:

1. Suitable signals must be given to enable pins of IC in order to enable the chip.
2. The order in which we are connecting the input variables to selection pins must be proper.

REAL TIME APPLICATIONS:

An 8×1 multiplexer (MUX) is used to select one data input out of many and send it to a single output line.

It is widely used in data routing, signal switching, and resource sharing in digital systems.

Applications include communication systems, microprocessor data selection, and memory management.

RESULT:

8X1 Mux by using 2X1 Mux is verified along with truth table.

VIVA QUESTIONS:

1. What is a multiplexer?
2. Which combinational circuit is renowned for selecting a single input from multiple inputs & directing the binary information to output line?
3. Which is the major functioning responsibility of the multiplexing combinational circuit?
4. How many select lines would be required for an 8-line-to-1-line multiplexer?
5. How many NOT gates are required for the construction of a 4-to-1 multiplexer?
6. What are the applications of multiplexer and de-multiplexer?
7. In 2n to 1 multiplexer how many selection lines are there?
8. How to get higher order multiplexers?
9. Implement an 8:1 mux using 4:1 muxes
10. What is the difference between multiplexer & demultiplexer?
11. Explain the operation of a digital multiplexer?
12. What makes the circuit of a multiplexer more complex?
13. What Is data selector?
14. What is a multiplexer?
15. Which mux without any additional circuitry can be used to obtain all the functions of 3 variable but not all of 4 variables?
16. How many 2*1 mux are required to realize 4*1 mux and explain how?
17. Design a 4*1 mux using 2*1 mux?
18. What are the minimum number of 21 mux required to generate 2 input nandgate and a 2 input Ex-OR gate?
19. How a multiplexer can act as a universal combinational circuit explain?
20. Construct a NOT gate using 2*1 mux
21. . Construct a AND gate using 2*1 mux
22. Construct OR gate using 2*1 mux with n-1 selection lines
23. Construct a NAND gate using 2*1 mux
24. Construct a NOR gate using 2*1 mux

25. Construct a Ex-OR gate using 2*1 mux
26. Construct a Ex-NOR gate using 2*1 mux
27. How many 2*1 mux are required for 8*1 mux construction?
28. How many 2*1 mux are required for 16*1 mux construction?
29. How many 2*1 mux are required for 64*1 mux construction?
30. Obtain the logic for the construction of different multiplexers using 2*1 mux?

Experiment No. 8

DESIGN AND REALIZATION OF 4 BIT COMPARATOR

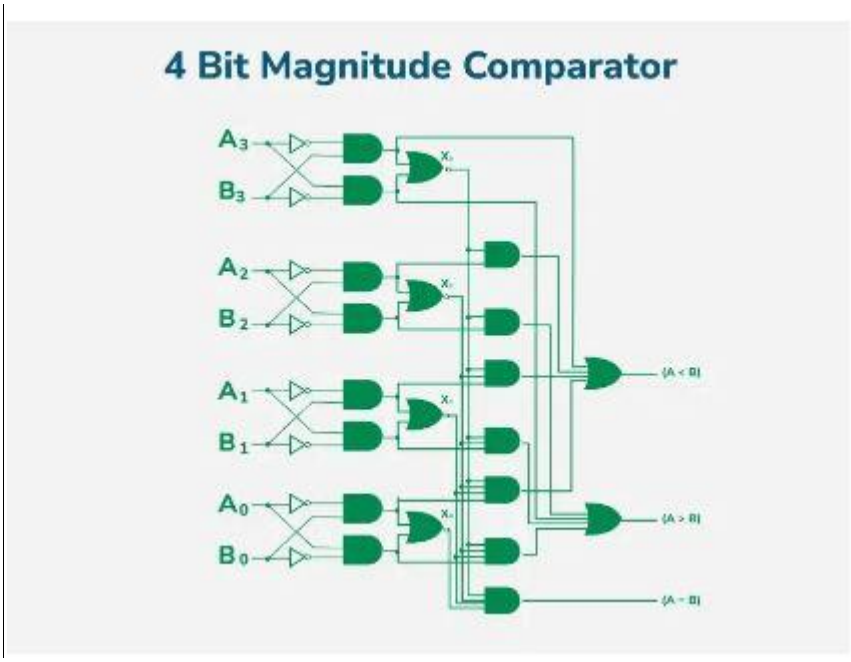
AIM:

Design and realization of 4 bit comparator

APPARATUS:

1. IC 7485
2. 4-BIT Digital Comparator Trainer Kit
3. Patch Cords

LOGIC DIAGRAM:



TRUTH TABLE:

A1	A0	B1	B0	A<B	A=B	A>B
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	0	1	0
1	0	1	1	1	0	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	0

THEORY:

A comparator used to compare two binary numbers each of two bits is called a 2-bit Magnitude comparator. It consists of four inputs and three outputs to generate less than, equal to, and greater than between two binary numbers.

PROCEDURE:

1) Connections are given as per circuit diagram
2) Logical inputs are given as per circuit diagram
3) Observe the output and verify the truth table

PRECAUTIONS:

1. The power supply pins must be checked whether power is available at those pins using test probes.
2. No loose connections should be there and care must be taken to avoid shorting of pins.

REAL TIME APPLICATIONS:

A 4-bit magnitude comparator is used to compare two binary numbers and determine their relative magnitude.

It is applied in digital sorting circuits, decision-making units, and arithmetic operations in computers.

Applications also include digital control systems, memory address decoding, and priority encoders.

RESULT:

Thus the design and implementation of magnitude comparator were done.s

VIVA QUESTIONS:

1. What is a magnitude comparator?
2. What is the purpose of a 2-bit comparator?
3. How many inputs does a 2-bit comparator have?
4. How many outputs does a 2-bit comparator have?
5. What do the outputs of a comparator indicate?
6. Define the output “A > B”.
7. Define the output “A = B”.
8. Define the output “A < B”.
9. Draw the truth table of a 2-bit comparator.
10. What logic gates are used in a 2-bit comparator?
11. How is equality detected in a 2-bit comparator?
12. How is A greater than B detected?
13. How is A less than B detected?
14. Can a 2-bit comparator be extended to 4 bits?
15. What is the Boolean expression for A > B?
16. What is the Boolean expression for A = B?
17. What is the Boolean expression for A < B?
18. Which flip-flop can be used to store the comparator output?
19. What is the significance of cascading comparators?
20. Give a real-time application of a 2-bit comparator.
21. How is a 2-bit comparator used in digital sorting?
22. Can a comparator be used in arithmetic circuits?
23. What is the difference between a 1-bit and 2-bit comparator?
24. Can the comparator be used in priority encoders?
25. Which IC is commonly used for magnitude comparison?
26. What happens if both inputs are equal?
27. What is the role of AND, OR, and NOT gates in a comparator?
28. How is a 2-bit comparator implemented using only NAND gates?
29. What is the speed limitation of a combinational comparator?
30. How is a 2-bit comparator tested in a lab experiment?

PART A: ELECTRONIC DEVICES LAB:

VIRTUAL LAB -1

VI Characteristics of a Diode

Aim of the experiment

At the end of the experiment, the student should be able to

- Explain the structure of a P-N junction diode
- Explain the function of a P-N junction diode
- Explain forward and reverse biased characteristics of a Silicon diode
- Explain forward and reverse biased characteristics of a Germanium diode

Procedure:

Forward Bias-Si Diode:

1. Set DC voltage to 0.2 V
2. Select the diode.
3. Set the resistor.
4. Voltmeter is placed parallel to Silicon diode and ammeter series with resistor.
5. The positive side of battery to the P side(anode) and the negative of battery to the N side(cathode) of the diode.
6. Now vary the voltage upto 5V and note the Voltmeter and Ammeter reading for particular DC voltage.
7. Take the readings and note Voltmeter reading across Silicon diode and Ammeter reading.
8. Plot the V-I graph and observe the change.
9. Calculate the dynamic resistance of the diode. rd=ΔV/ΔI
10. Therefore from the graph we see that the diode starts conducting when the forward bias voltage exceeds around 0.6 volts (for Si diode). This voltage is called cut-in voltage.

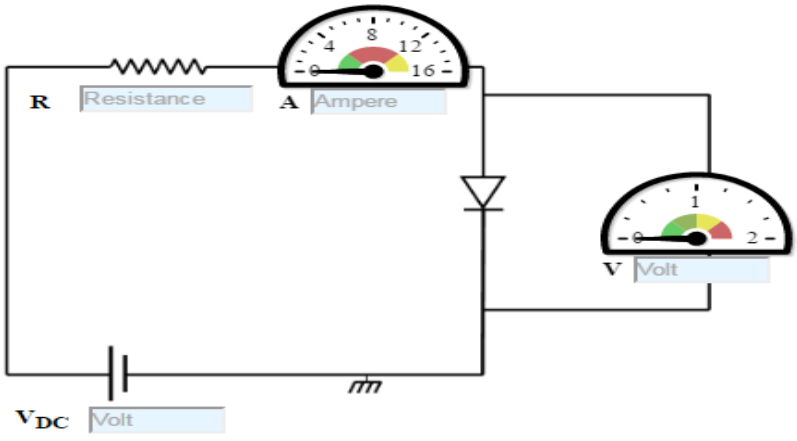


Figure:1

Reverse Bias-Si Diode:

1. Set DC voltage to 0.2 V .
2. Select the diode.
3. Set the resistor.
4. Voltmeter is placed parallel to Silicon diode and ammeter series with resistor.
5. The positive terminal of battery is connected to the N side(cathode) and the negative terminal of battery is connected to the P side(anode) of a diode.
6. Now vary the voltage upto 30V and note the Voltmeter and Ammeter reading for DC voltage .
7. Take the readings and note Voltmeter reading across Silicon diode and Ammeter reading.
8. Plot the V-I graph and observe the change.

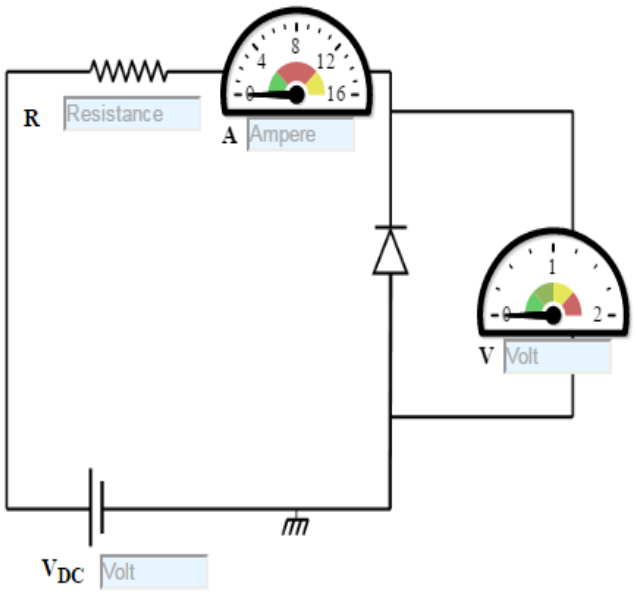


Figure: 2

Forward Bias-Ge Diode:

1. Set DC voltage to 0.2 V
2. Use the resistor of 1K ohms and a Germanium diode.
3. Voltmeter is placed parallel to Germanium diode and ammeter series with resistor.
4. The positive terminal of battery is connected to the P side(anode) and the negative terminal of battery is connected to the N side(cathode) of the diode.
5. Now vary the voltage upto 30V and note the Voltmeter and Ammeter reading for particular DC voltage .
6. Take the readings and note Voltmeter reading across Germanium diode and Ammeter reading.
7. Plot the V-I graph and observe the change.
8. Therefore from the graph we see that the diode starts conducting when the forward bias voltage exceeds around 0.3 volts (for Ge diode). This voltage is called cut-in voltage.

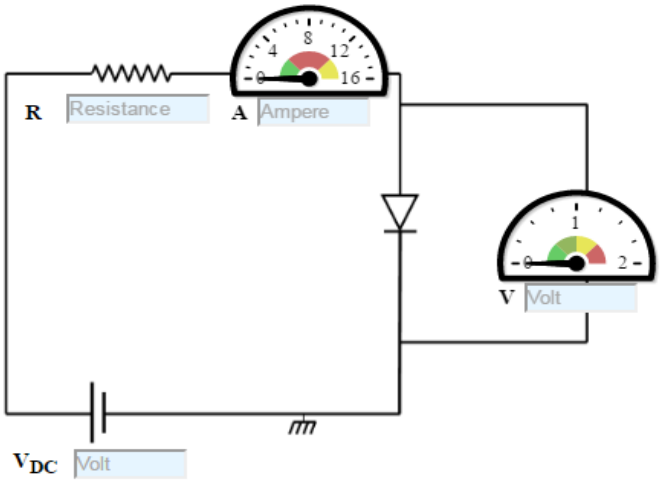


Figure: 3

Reverse Bias-Ge Diode:

1. Set DC voltage to 0.2 V
2. Use the resistor of 1K ohms and a Germanium diode.
3. Voltmeter is placed parallel to Germanium diode and ammeter series with resistor.
4. The positive terminal of battery is connected to the N side(cathode) and the negative terminal of battery is connected to the P side(anode) of a diode.
5. Now vary the voltage upto 30V and note the Voltmeter and Ammeter reading for DC voltage
6. Take the readings and note Voltmeter reading across Silicon diode and Ammeter reading.
7. Plot the V-I graph and observe the change.

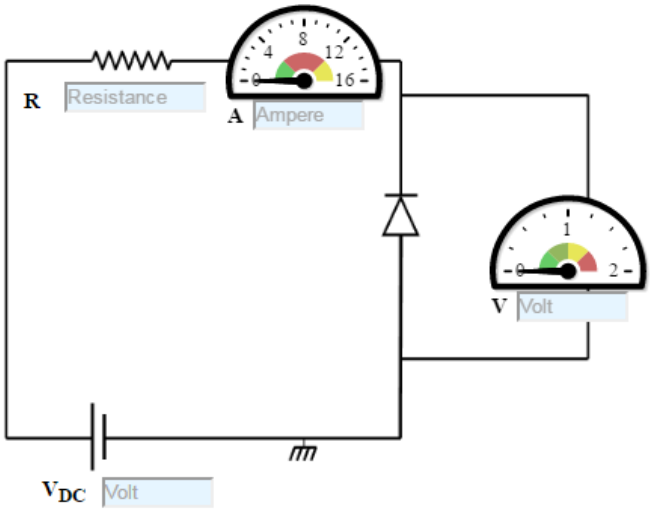


Figure: 4

Url: **https://be-iitkgp.vlabs.ac.in/exp/characteristics-diode/**

Conclusion: The V–I characteristics of a diode show that it conducts current in forward bias after the cut-in voltage and offers low resistance. In reverse bias, it allows only a small leakage current, confirming its unidirectional behavior.

VIRTUAL LAB -2

Zener Diode-Voltage Regulator

Aim of the experiment:

At the end of the experiment, the student will be able to

- Explain the function of a Zener diode
- Explain Zener Diode as Voltage Regulator

Procedure

Zener Diode - Line Regulation

1. Set the Zener Voltage(V_Z)
2. Set the Series Resistance (R_S) value.
3. Set the Load Resistance (R_L) value.
4. Vary DC voltage.
5. Voltmeter is placed parallel to load resistor and ammeter series with the series resistor.
6. Choose appropriate DC voltage such that zener diode is 'on'.
7. Now note the Voltmeter and Ammeter reading for various DC voltage.
8. Note the Load current(I_L), zener current(I_Z), Output voltage(VO)
9. Calculate the voltage regulation.

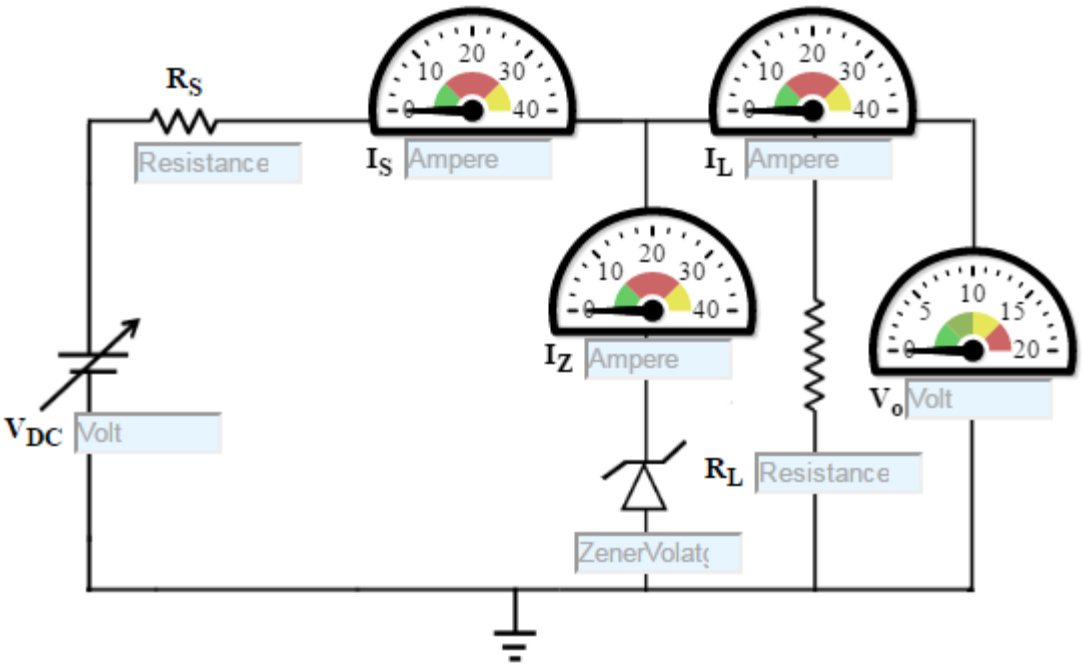


Figure:1

Zener Diode - Load Regulation

1. Set DC voltage.
2. Set the Series Resistance (R_S) value.
3. 1W D0-41 Glass Zener Diode 1N4740A, Zener voltage is 10 V.
4. Vary the Load Resistance (R_L).
5. Voltmeter is placed parallel to load resistor and ammeter series with the series resistor.
6. Choose Load Resistance in such a manner, such that the Zener diode is 'on'.
7. Now note the Voltmeter and Ammeter reading for various Load Resistance.
8. Increase the load resistance (R_L).
9. Note the Load current (I_L), zener current (I_Z), Output voltage(VO)
10. Calculate the voltage regulation.

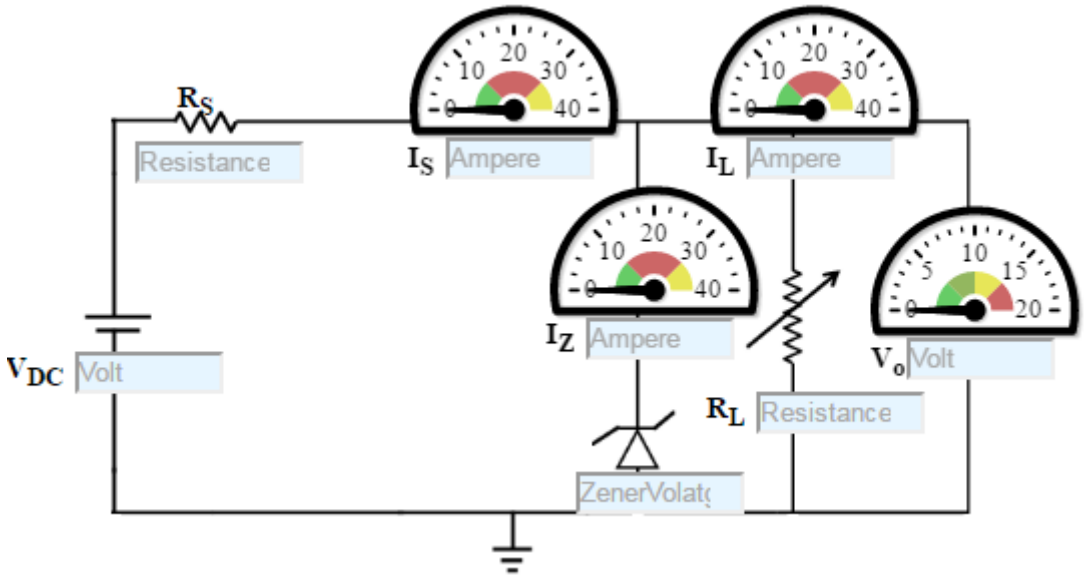


Figure:2

Zener Characteristics

1. Select the diode
2. Set the rheostat Rh=1 Ω
3. By adjusting the rheostat, voltmeter reading is increased from 0 and in each time note the corresponding reading in milliammeter.
4. Take the readings and note Voltmeter reading across Zener diode and Ammeter reading.
5. Plot the V-I graph and observe the change.

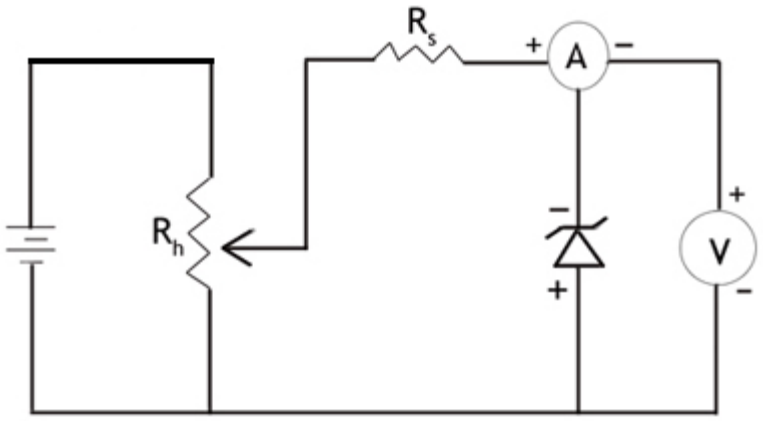


Figure: 3

Url: https://be-iitkgp.vlabs.ac.in/exp/voltage-regulator/index.html

Conclusion:

The Zener diode was studied for its voltage regulating characteristics in the reverse bias region. From the experiment, it is observed that when the reverse voltage reaches the Zener breakdown voltage, the diode maintains a nearly constant voltage across it even if the current changes. This property makes the Zener diode very useful as a voltage regulator in electronic circuits.

VIRTUAL LAB -3

Full Wave Rectification

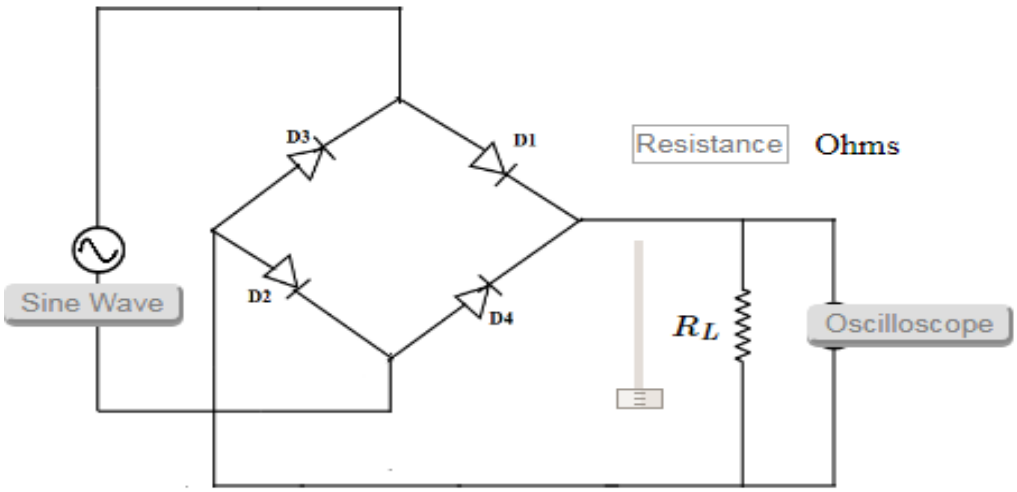
Aim of the experiment:

At the end of the module the student would be able to

- Explain Rectification
- Explain center Tapped Full Wave Rectification
- Explain Bridge Full Wave Rectification

Procedure:

1. Set the resistor R_L.
2. Click on 'ON' button to start the experiment.
3. Click on 'Sine Wave' button to generate input waveform
4. Click on 'Oscilloscope' button to get the rectified output.
5. Vary the Amplitude, Frequency, volt/div using the controllers.
6. Click on "Dual" button to observe both the waveform.
7. Channel 1 shows the input sine waveform, Channel 2 shows the output rectified waveform.
8. Calculate the Ripple Factor.Theoretical Ripple Factor= 0.483.



Url: https://be-iitkgp.vlabs.ac.in/exp/full-wave-rectification/procedure.html

Conclusion:

The full wave rectifier converts both half cycles of the AC input into a pulsating DC output, resulting in higher efficiency compared to half-wave rectification.

It provides better output voltage, lower ripple factor, and improved utilization of the transformer.

VIRTUAL LAB -4

BJT Common Emitter Characteristics

Aim of the experiment:

At the end of the module the student would be able to explain

- Explain structure of Bipolar Junction Transistor
- Explain Operation of Bipolar Junction Transistor
- Explain Common Emitter characteristics of a BJT

Procedure:

BJT Common Emitter - Input Characteristics:

1. Initially set rheostat R_{h1} = 1 Ω and rheostat R_{h2} = 1 Ω
2. Set the Collector-Emitter Voltage(V_{CE}) to 1 V by adjusting the rheostat R_{h2}
3. Base Emitter Voltage(V_{BE}) is varied by adjusting the rheostat R_{h1}.
4. Note the reading of Base current(I_B)in micro Ampere.
5. Click on 'Plot' to plot the I-V characteristics of Common-Emitter configuration. A graph is drawn with V_{BE} along X-axis and I_B along Y-axis.
6. Click on 'Clear' button to take another sets of readings
7. Now set the Collector-Emitter Voltage(V_{CE}) to 2 V, 3 V, 4 V

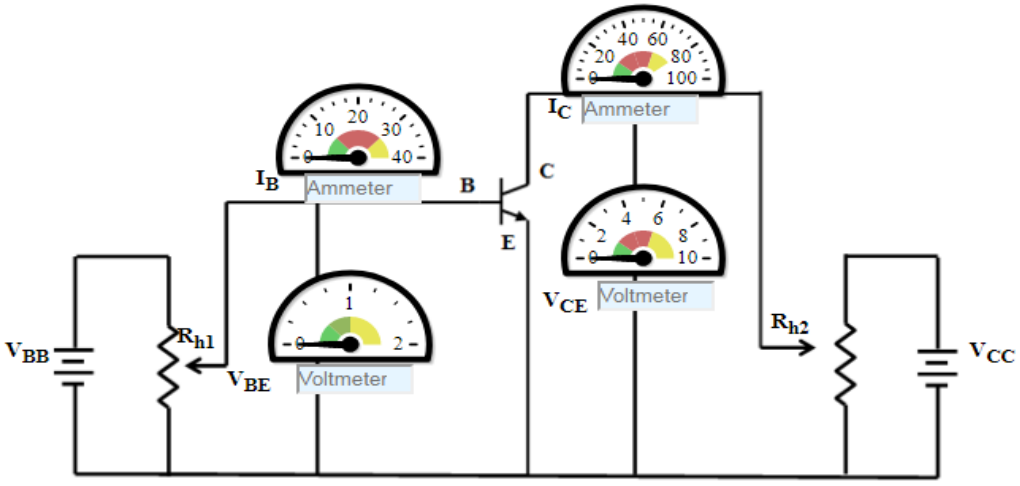


Figure:1

BJT Common Emitter - Output Characteristics:

1. Initially set rheostat R_{h1} = 1 Ω and rheostat R_{h2} = 1 Ω
2. Set the Base current(I_B)15 uA by adjusting the rheostat R_{h1}
3. Vary the Collector-Emitter Voltage(V_{CE})is varied by adjusting the rheostat R_{h2}.
4. Note the reading of Collector current(I_C).
5. Click on 'Plot' to plot the I-V characteristics of Common-Emitter configuration. A graph is drawn with V_{CE} along X-axis and I_C along Y-axis.
6. Click on 'Clear' button to take another sets of readings
7. Now set the Base Current(I_B) to 20 uA

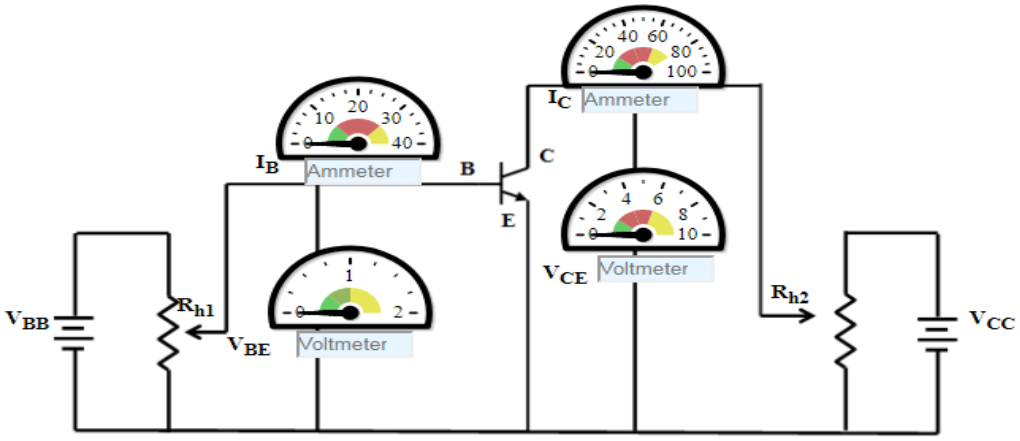


Figure: 2

Url: **https://be-iitkgp.vlabs.ac.in/exp/common-emitter-characteristics/index.html**

Conclusion:

The common emitter configuration of a BJT provides high current and voltage gain, making it suitable for amplification.

The characteristics show that collector current is controlled by base current, and the circuit exhibits moderate input resistance and high output resistance.

PART-B: DIGITAL ELECTRONICS

VIRTUAL LAB -1

Analysis and Synthesis of Boolean Expressions using Basic Logic Gates

Aim of the experiment:

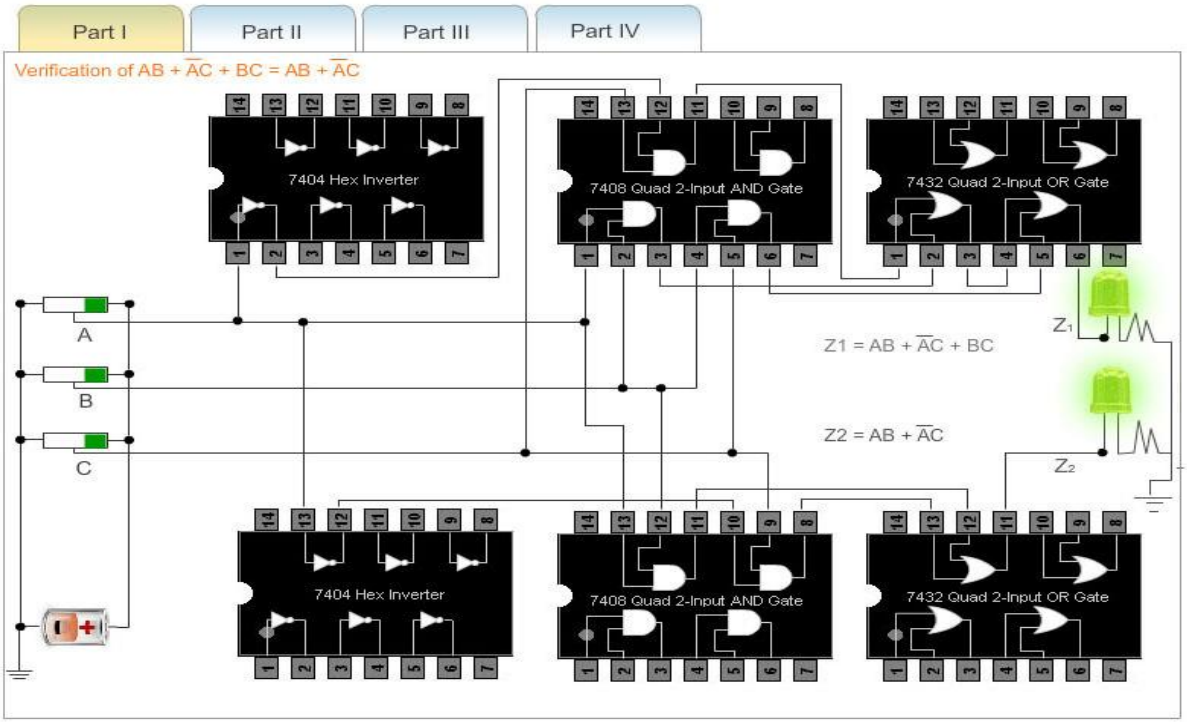
The principal objective of this experiment is to fully understand the function and use of logic gates such as 7400(quad 2-input NAND gates),7402(quad 2-input NOR gates),7404(Hex inverter) 7408(quad 2-input AND gates) and 7432(quad 2-input OR gates).

Procedure:

Please follow these steps to do the experiment.

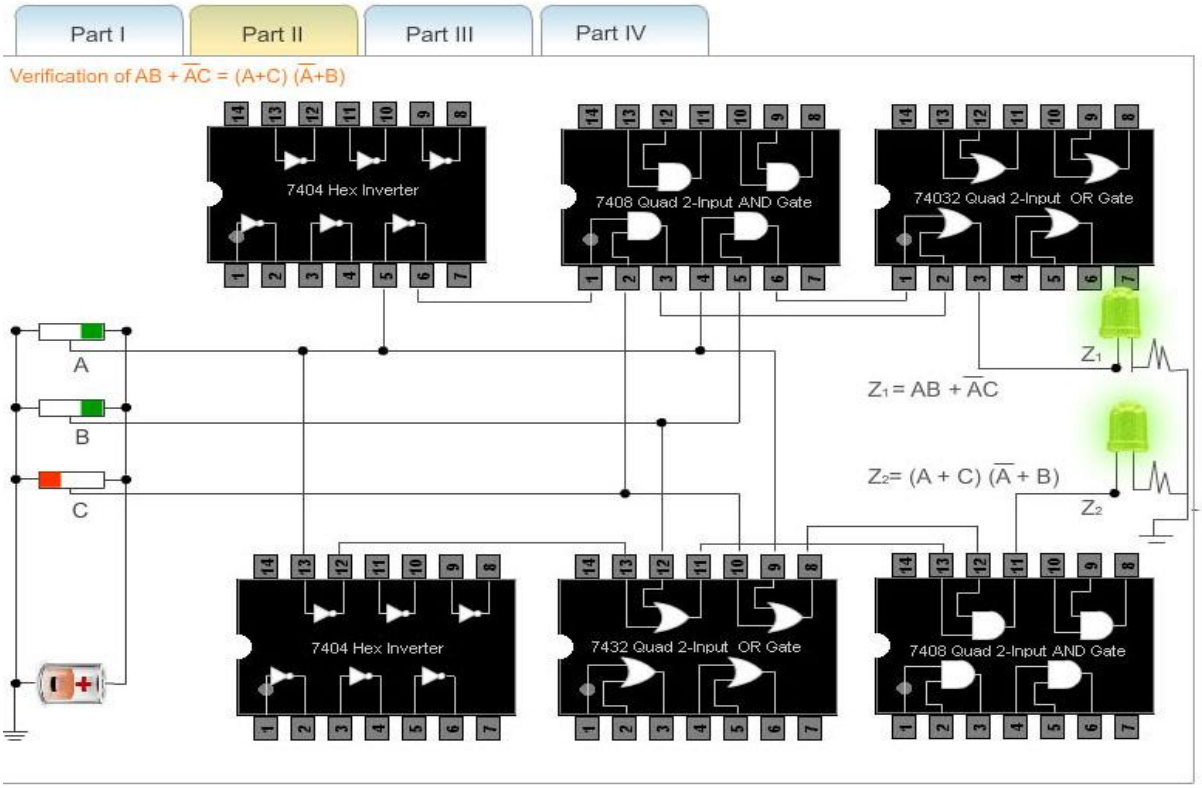
Part 1:

1. At first go through the structure of 7404 Hex inverter, 7408(quad 2-input AND gates), 7432(quad 2-input OR gates).
2. Next, apply a high level voltage to all the inputs A,B,C.
3. Next, check that both LEDs glow. This is because both the outputs z1 and z2 attain the same value.
4. Thus, AB+AC+BC=AB+AC holds for the condition A=B=C="1".
5. For all the combinations of the variables A,B, and C verify that both the LEDs are glowing or not glowing. If the LED glows, it indicates that the corresponding output has reached logic 1 level. Similarly a dark LED indicates low level output voltage.



Part 2:

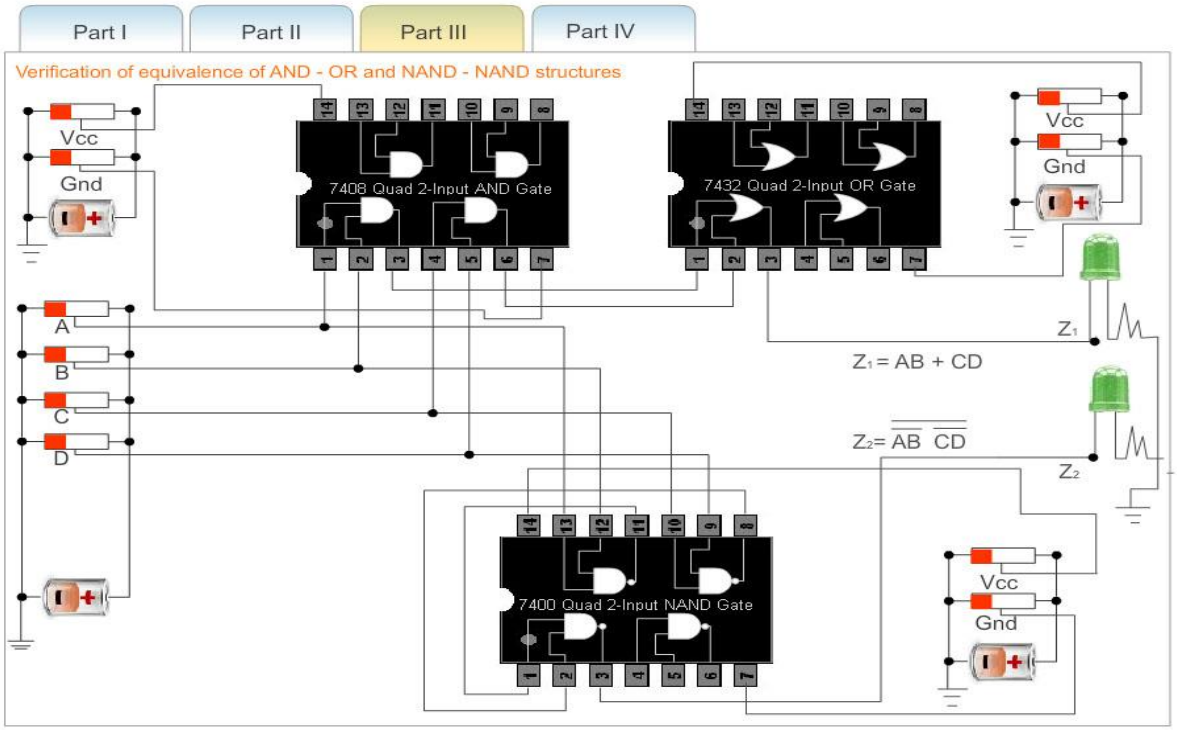
1. At first go through the structure of 7400(quad 2-input NAND gates), 7408(quad 2-input AND gates), 7432(quad 2-input OR gates).
2. Next, apply a high level voltage to inputs A,B.and apply low level voltage to the input C.
3. Next, check that both LEDs glow. This is because both the outputs z1 and z2 attain the same value.
4. So, the equivalence of AND-OR and NAND NAND structure can be verified.
5. For all the combinations of the variables A,B and C verify that both the LEDs are glowing or not glowing. If the LED glows, it indicates that the corresponding output has reached logic 1 level. Similarly a dark LED indicates low level. output voltage.

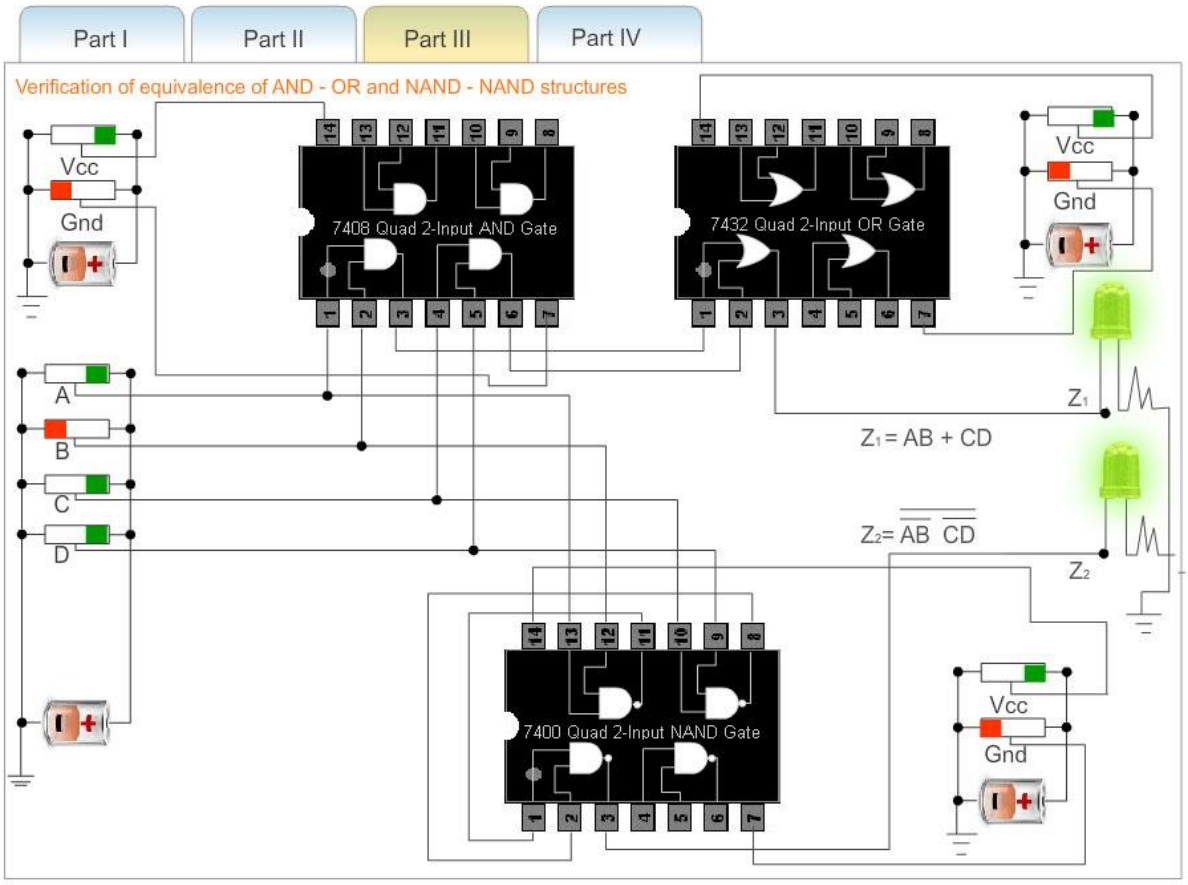


Part 3:

1. At first go through the structure of 7404 Hex inverter, 7408(quad 2-input AND gates), 7432(quad 2-input OR gates), 7400(quad 2-input NAND gates).
2. Next, apply a high level voltage to all the Vcc inputs and keep low level voltage to all the Gndinputs.IfVcc and ground are not connected properly then error message will be appeared and no output will be generated.
3. Next, apply a high level voltage to the inputs A,B and apply low level voltage to the input C.
4. Next, check that both LEDs glow.This is because both the outputs z1 and z2 attain the same value.
5. Thus, AB+AC+BC=AB+AC =(A+C)(A+B) holds for the condition A=B="1" and C=D="0"

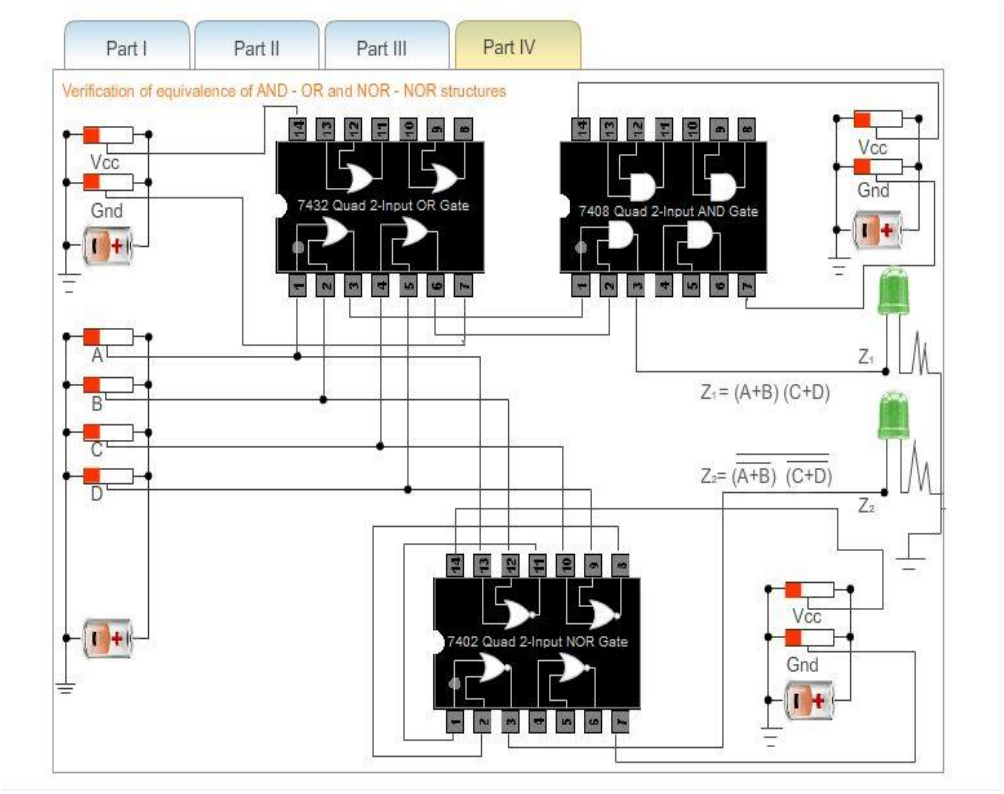
6. For all the combinations of the variables A,B and C verify that both the LEDs are glowing or not glowing. If the LED glows, it indicates that the corresponding output has reached logic 1 level. Similarly a dark LED indicates low level output voltage

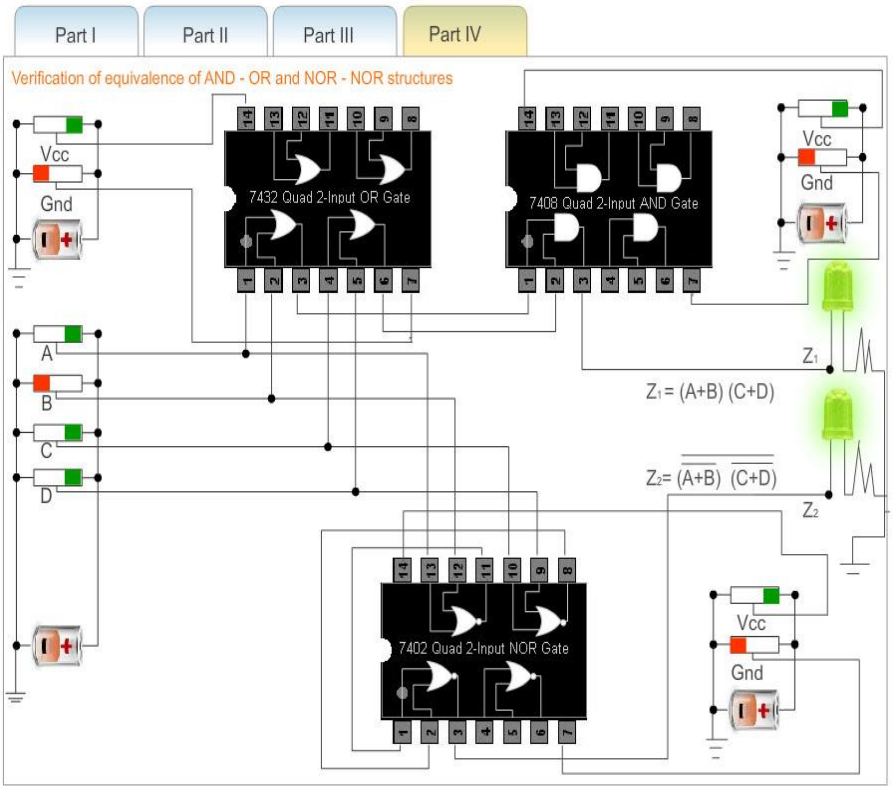




Part 4:

1. At first go through the structure of 7402(quad 2-input NOR gates), 7408(quad 2-input AND gates), 7432(quad 2-input OR gates).
2. Next, apply a high level voltage to all the Vcc inputs and apply low level voltage to all the Gndinputs.IfVcc and ground are not connected properly then error message will be appeared and no output will be generated.
3. Next, apply a high level voltage to all the inputs A,C and apply low level voltage to the inputs B,D.
4. Next, check that both LEDs glow.This is because both the outputs z1 and z2 attain the same value.
5. So, the equivalence of OR-AND and NOR-NOR structure can be verified.
6. For all the combinations of the variables A,B,C and D verify that both the LEDs are glowing or not glowing. If the LED glows, it indicates that the corresponding output has reached logic 1 level. Similarly a dark LED indicates low level output voltage.





Url: **https://dec-iitkgp.vlabs.ac.in/exp/basic-logic-gates/**

Conclusion:

The experiment demonstrates that Boolean expressions can be effectively analyzed and simplified using Boolean algebra and implemented using basic logic gates.

Thus, the required logical function is successfully synthesized, confirming the correctness of the Boolean expression and gate-level realization.

VIRTUAL LAB -2

Generation of clock using NAND/NOR gates

Aim: To design a clock generator using NAND gate

Procedure:

1. Click on the **Component** button to place components on the table.

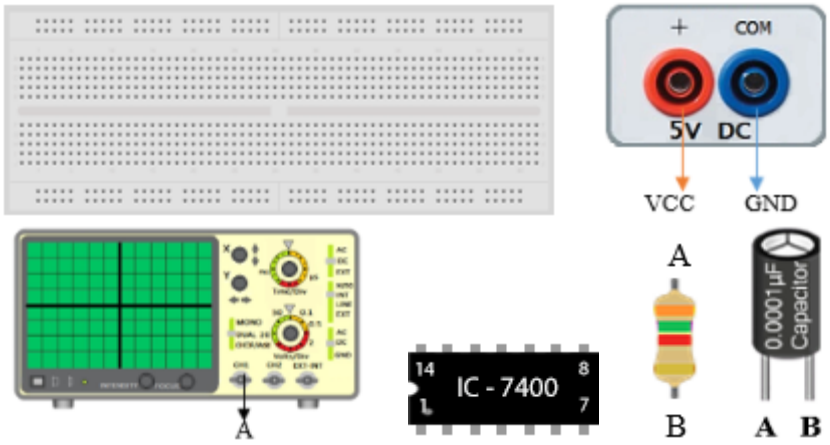


Fig. 1 Components

2. Make connections as per the circuit diagram and pin diagram of IC or according to connection table.
3. Connect the C.R.O on output terminal of circuit (Refer connection table).

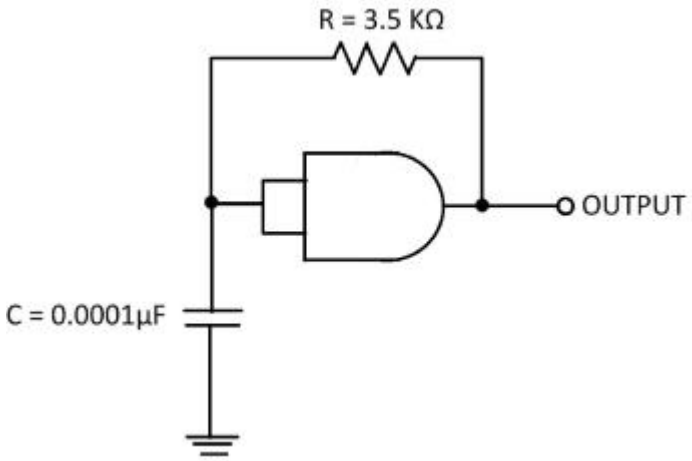


Fig. 2 Circuit diagram of clock pulse using NAND gate

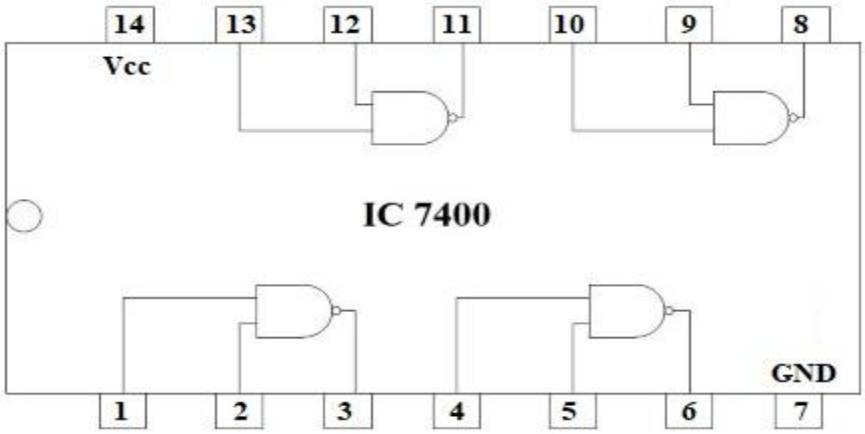


Fig. 3 Pin diagram of IC 7400

Table 1: Connection table

S. No.	Source	Target
1	IC7400 _ Terminal 14	Supply VCC
2	IC7400 _ Terminal 07	Supply VCC
3	Capacitor (C) _ Terminal A	Supply GND
4	Capacitor (C) _ terminal B	Resistance (R_1) _ Terminal A
5	Capacitor (C) _ Terminal B	IC7400 _ Terminal 13
6	Capacitor (C) _ Terminal B	IC7400 _ Terminal 12
7	Resistance (R_1) _ Terminal B	IC7400 _ Terminal 11
8	IC7400 _ Terminal 11	CRO _ Terminal A

4. Click on **Check Connections** button. If connections are right, click on **'OK'**, then **Simulation** will become active.
5. Connect CH1/CH2 of C.R.O. to output terminal of the circuit.
6. Observe output wave on C.R.O by adjusting C.R.O channel **CH1/CH2** and **TIME** knobs.
7. Use **X** Shift and **Y** Shift buttons for wave shifting.
8. Measure the time period of output wave at C.R.O. and calculate the frequency by feeding the time period in the given box.
9. Compare both experimental and theoretical frequencies.
10. Click on the **Reset** button to reset the page.

Url: https://ade-iitr.vlabs.ac.in/exp/generation-of-clock/procedure.html

Conclusion :

The experiment on generation of clock pulses using NAND gates was successfully performed. It is observed that by connecting NAND gates with suitable RC components, a periodic square wave (clock signal) can be generated. The circuit operates as an astable multivibrator, continuously switching between logic HIGH and logic LOW states without any external triggering.

VIRTUAL LAB -3

Analysis and Synthesis of Arithmetic Expressions using Adders/Subtractors

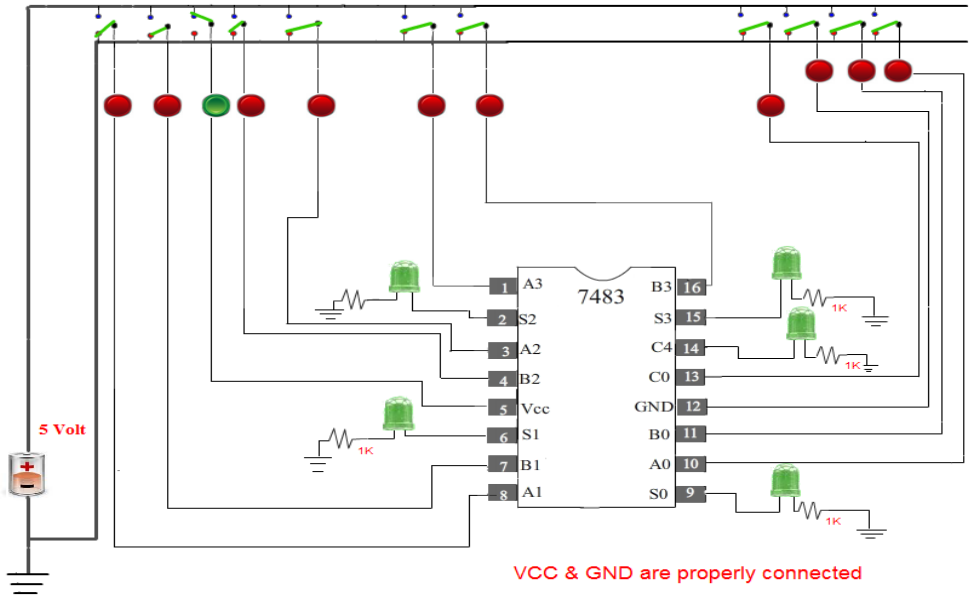
Aim of experiment:

- The objective of part 1 of the experiment is to fully understand the functionality of 4 bit binary full adder.
- The objective of part 2 of the experiment is to fully understand the functionality of 8 bit full adder by cascading to 7483 chips(two 4 bit full adder).
- The objective of part 3 of the experiment is to fully understand the functiponality and implementation of 4 bit adder/subtractor

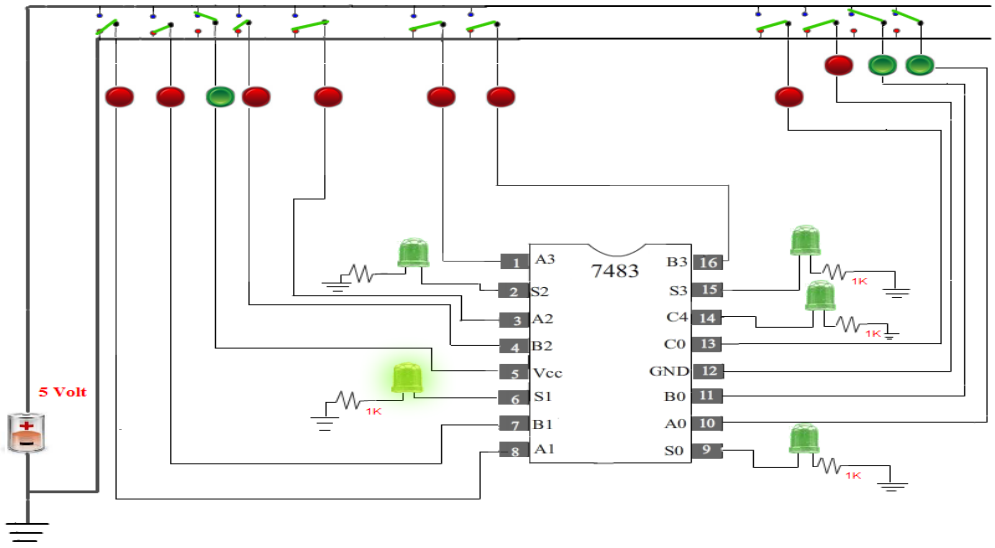
Procedure:

Please follow these steps to do the experiment:

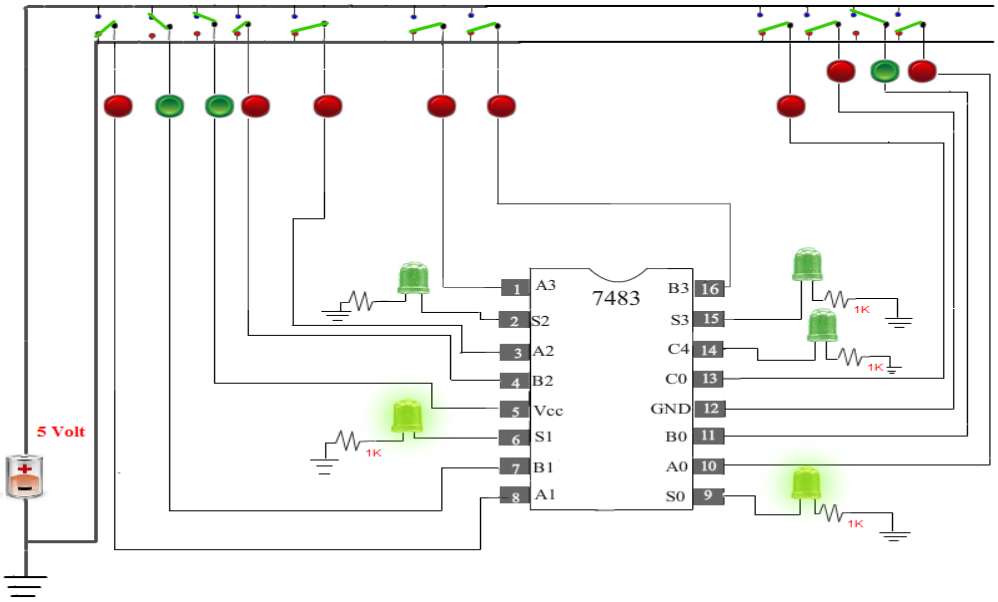
1. At first click on the V_{cc} switch that means V_{cc} = 1 and GND = 0 , show message Vcc& GND properly connected.



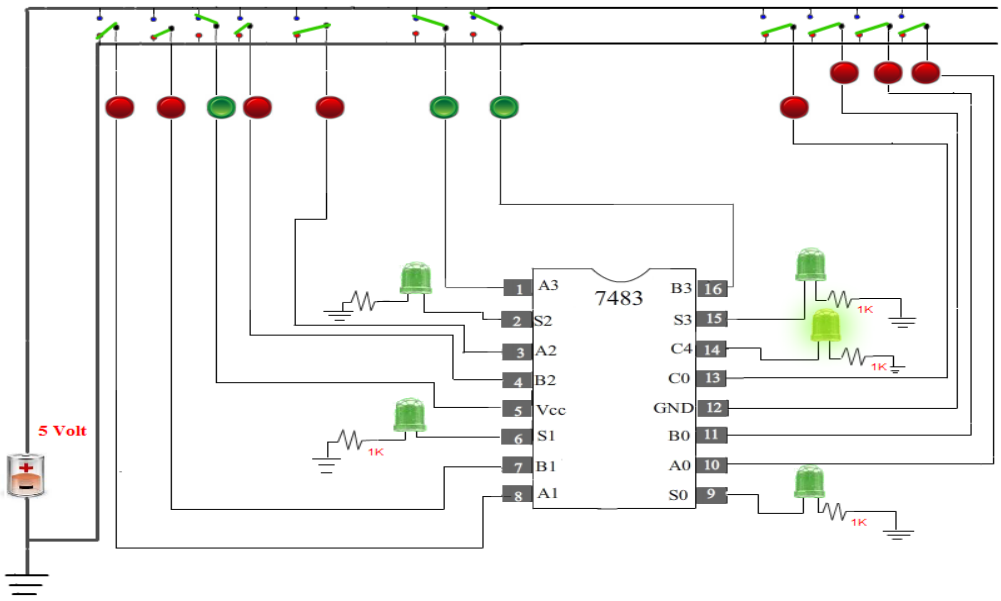
2. Next, A_0= 1, A_1= 0, A_2= 0, A_3= 0 and B_0= 1, B_1= 0, B_2= 0, B_3= 0 now you can see the output result of S_0= 0, S_1= 1, S_2= 0, S_3= 0 and C_4= 0.



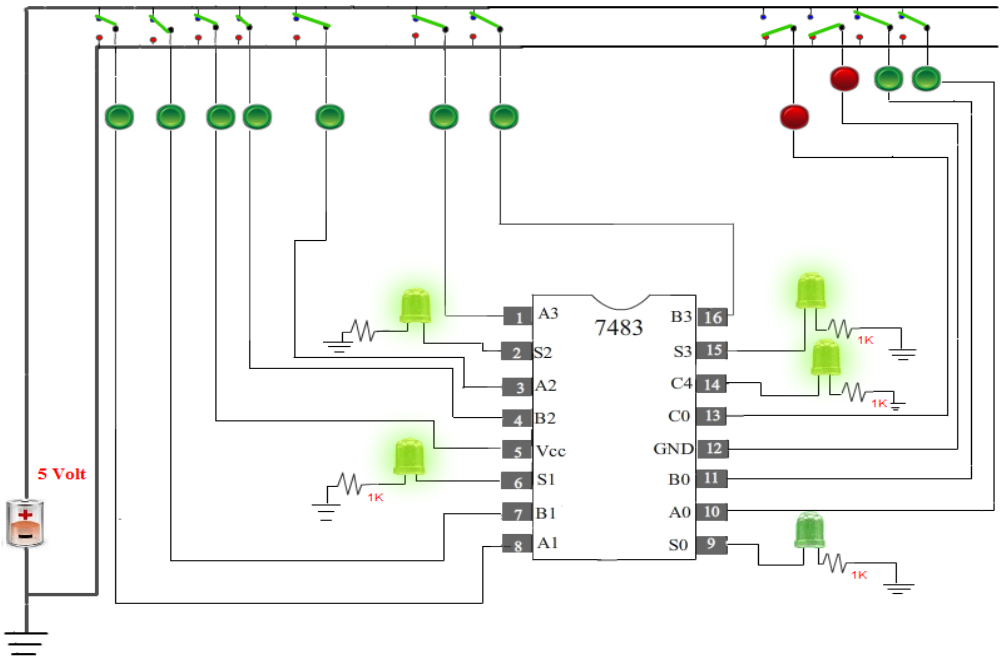
3. Next, A_0= 0, A_1= 0, A_2= 0, A_3= 0 and B_0= 1, B_1= 1, B_2= 0, B_3= 0 now you can see the output result of S_0= 1, S_1= 1, S_2= 0, S_3= 0 and C_4= 0.



4. Next, A_0= 0, A_1= 0, A_2= 0, A_3= 1 and B_0= 0, B_1= 0, B_2= 0, B_3= 1 now you can see the output result of S_0= 0, S_1= 0, S_2= 0, S_3= 0 and C_4= 1.



5. Next, A_0= 1, A_1= 1, A_2= 1, A_3= 1 and B_0= 1, B_1= 1, B_2= 1, B_3= 1 now you can see the output result of S_0= 0, S_1= 1, S_2= 1, S_3= 1 and C_4= 1.



Url: https://dec-iitkgp.vlabs.ac.in/exp/arithmetic-expressions/

Conclusion:

The experiment confirms that arithmetic expressions can be correctly analyzed and implemented using adders and subtractors.

The designed circuits perform accurate addition and subtraction operations, validating the logical design and functionality of arithmetic circuits.

VIRTUAL LAB -4

AIM: To analyze the truth table of binary to gray and gray to binary converter using combination of NAND gates and to understand the working of binary to gray and gray to binary converter with the help of LEDs display.

Gray to Binary Conversion

Step-1) Connect battery to supply 5V to the circuit.

Step-2) Press Switches for different inputs.

The switch in ON state is and the switch in OFF state is

Step-3) The corresponding combination of input and output LEDs lit up for different combination of inputs.

The input gray code LEDs are G3,G2,G1 and G0 and the output binary code LEDs B3,B2,B1 and B0 glow accordingly.

The input LED in OFF state is and in ON state is .

The output LED in OFF state is and in ON state is .

Step-4) Click "Add" to add the values to the Truth Table.

Step-5) Click "Print" to get the print out of the Truth Table.

Binary to Gray Code Conversion

Step-1) Connect battery to supply 5V to the circuit.

Step-2) Press Switches for different inputs.

The switch in ON state is and the switch in OFF state is

Step-3) The corresponding combination of input and output LEDs lit up for different combination of inputs.

The input binary code LEDs are B3,B2,B1 and B0 and the output gray code LEDs G3,G2,G1 and G0 glow accordingly.

The input LED in OFF state is and in ON state is .

The output LED in OFF state is and in ON state is .

Step-4) Click "Add" to add the values to the Truth Table.

Step-5) Click "Print" to get the print out of the Truth Table.

Url: https://de-iitr.vlabs.ac.in/exp/binary-conversion/index.html

Conclusion :

The experiment on Binary to Gray (BTOG) and Gray to Binary (GTOB) code conversion was successfully carried out using logic gates. From the results obtained, it is observed that the binary number can be correctly converted into its corresponding Gray code and vice versa.

VIRTUAL LAB -5

Analysis and Synthesis of Multi-bit Sequential Circuits using Shift Registers

Aim of experiment:

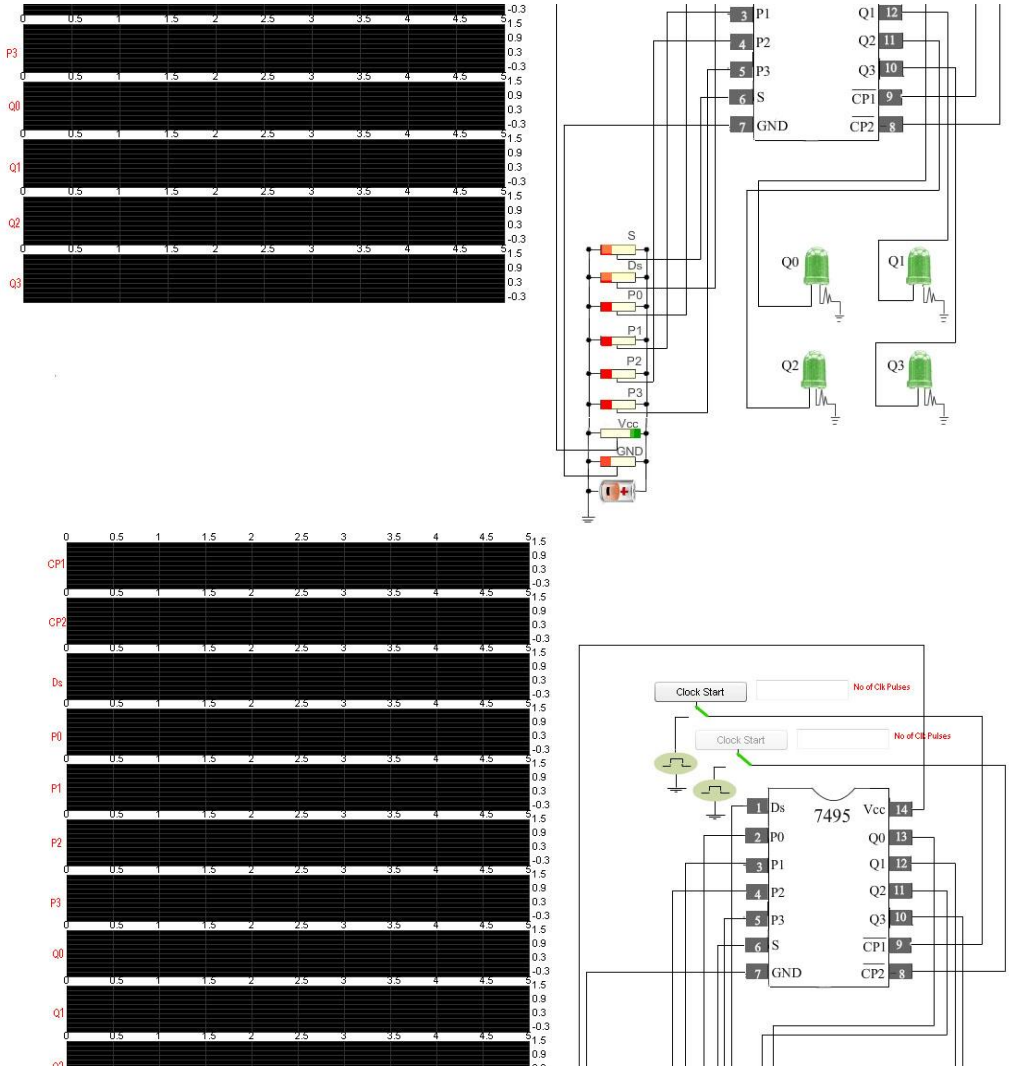
The objective of the experiment is to fully understand the functionality of 4-bit Shift Register using SN54/74LS95B which has two separate clock inputs, one for shifting operation and other is for parallel loading operation. These two operations are controlled by a mode control input

Procedure:

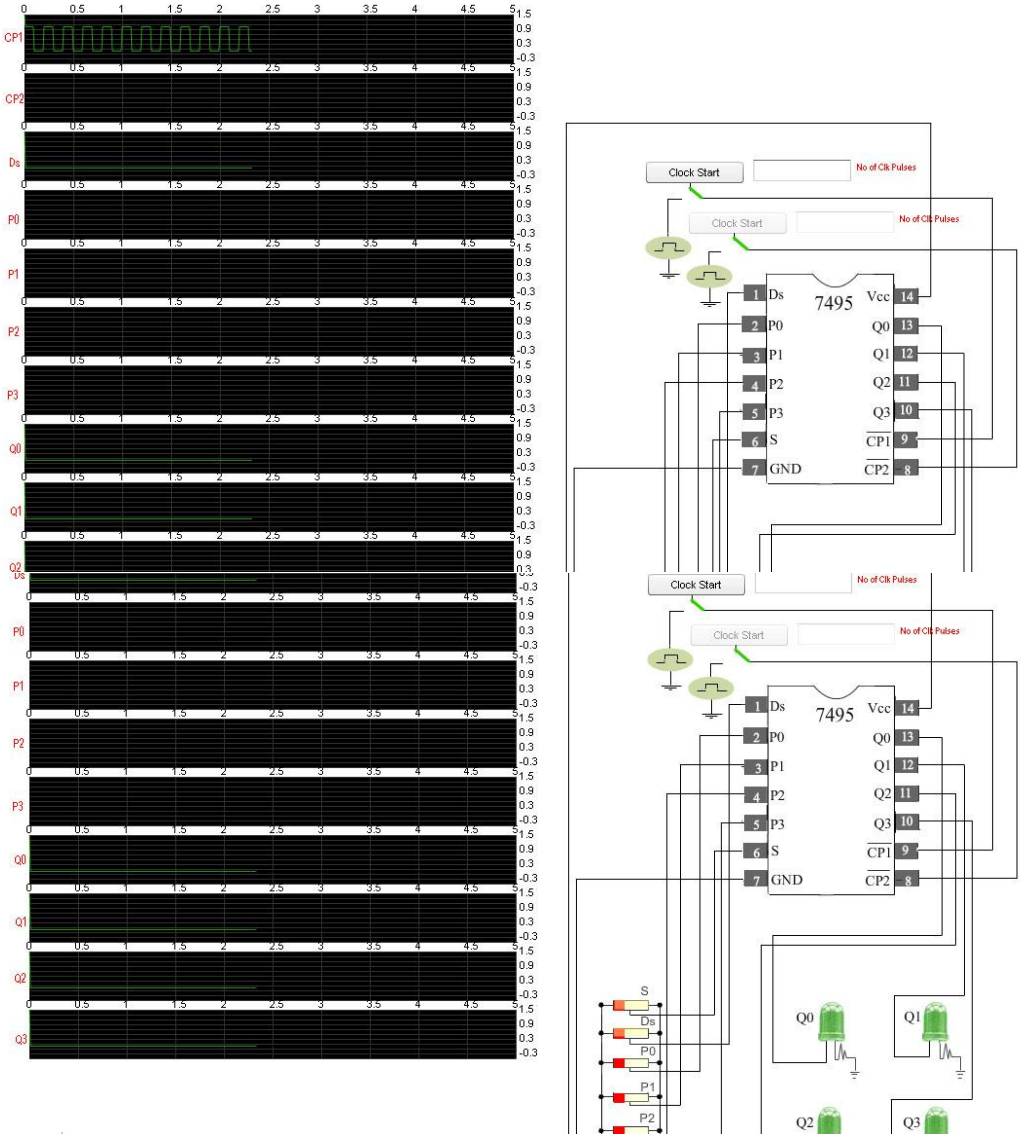
Please follow these steps to do the experiment.

Part 1:

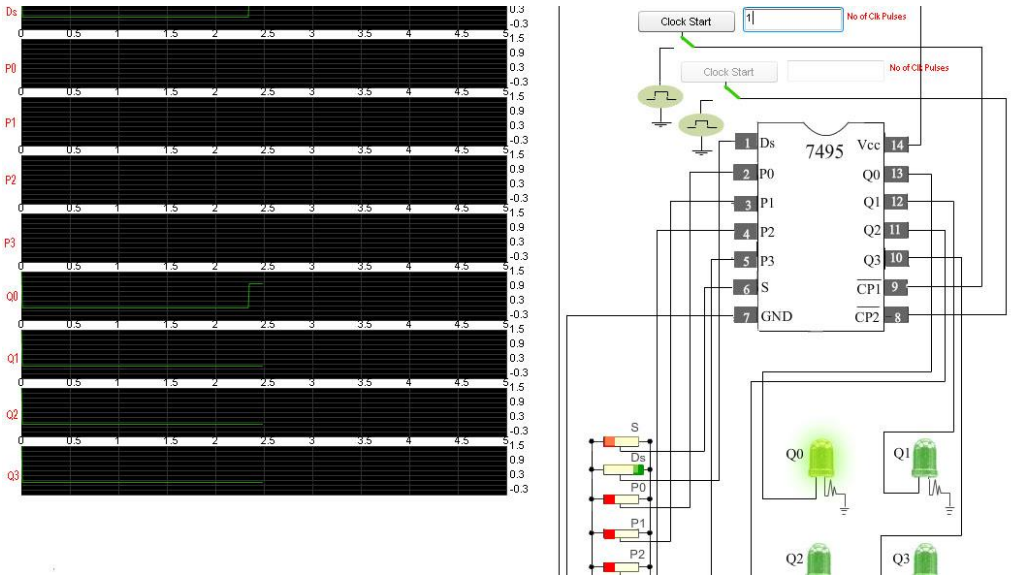
1. At first apply high voltage to V_{cc}.So that the "Clock Start" button for the clock pulse(CP1) will be enabled.



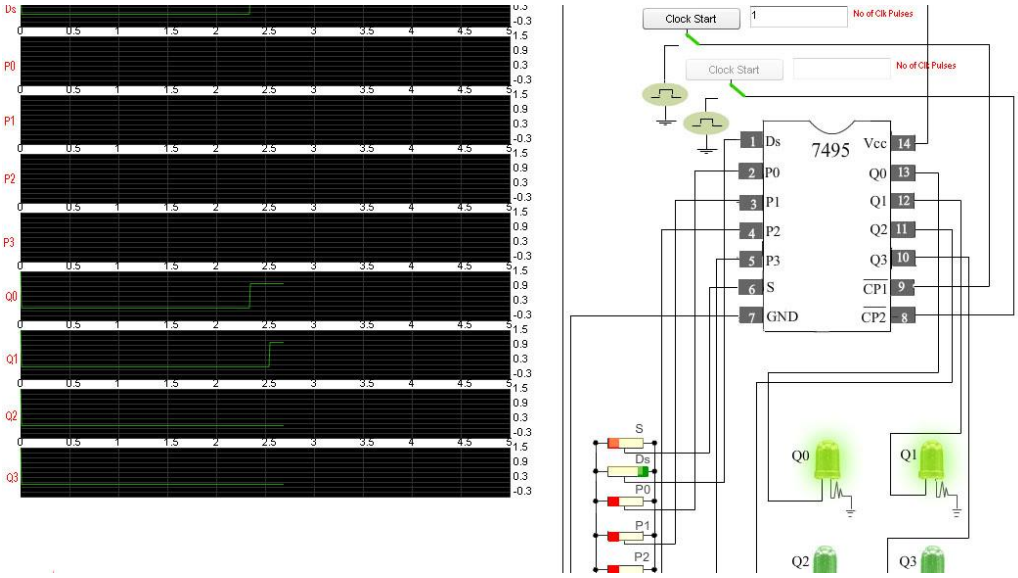
2. Next, apply low voltage to the mode control input (S) and start the clock pulse(CP1).Now the serial input D_s is enabled.The input at D_s will be shifted right to the outputs Q_0, Q_1, Q_2, Q_3 at negetive transition of CP1.All the parallel inputs P_0, P_1, P_2, P_3 are disabled



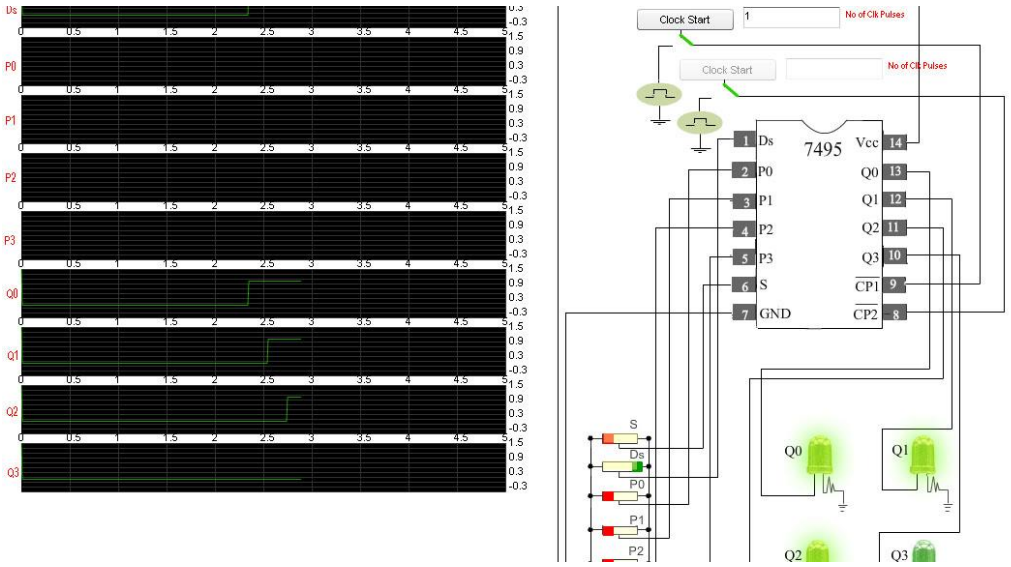
3. Now apply high voltage to D_s input and set no of clock pulses to 1.See that the input will be shifted to Q_0 output at negetive clock edge.



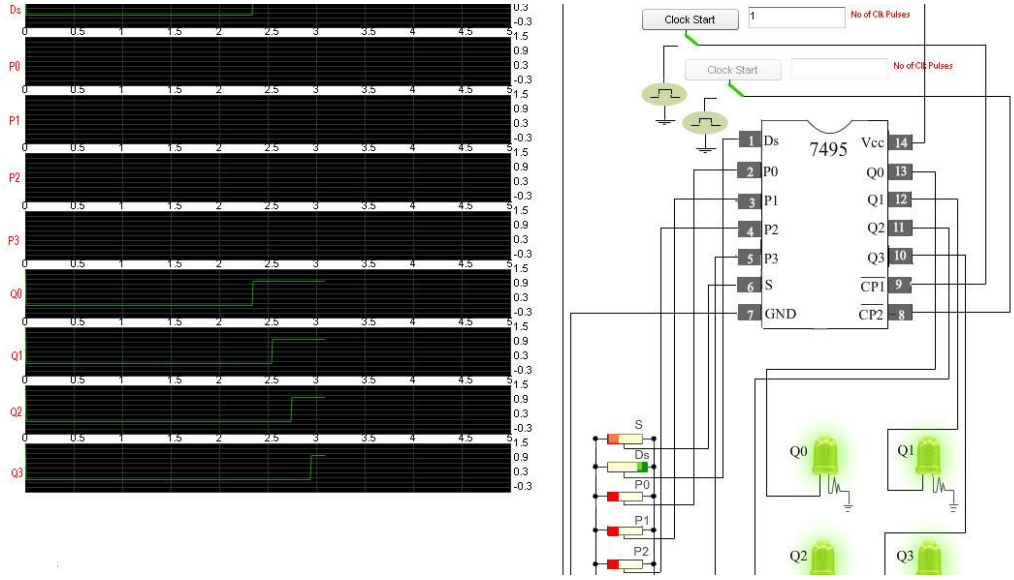
4. Next, start the clock pulse again.See the input is now shifted to the output Q_1.



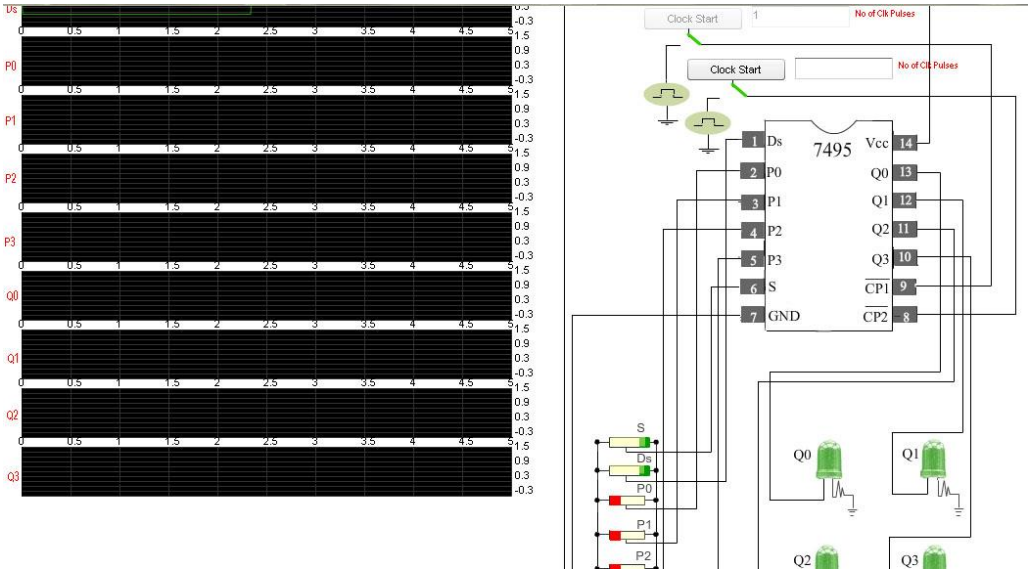
5. Again start the clock pulse and see the input is shifted to the output Q_2.



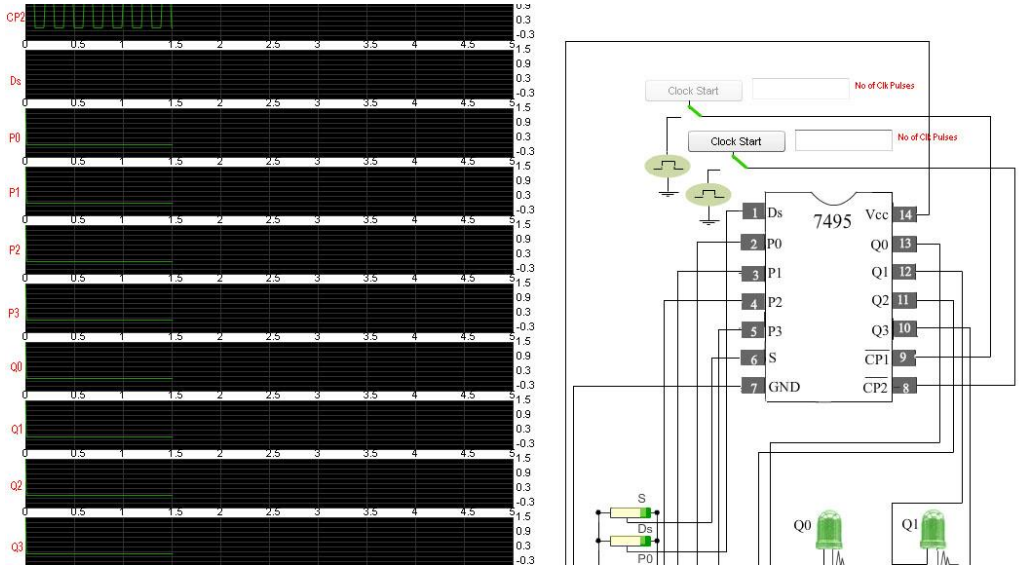
6. Start the clock pulse again.Now see that at fouth clock pulse input is shifted to the output Q_3.



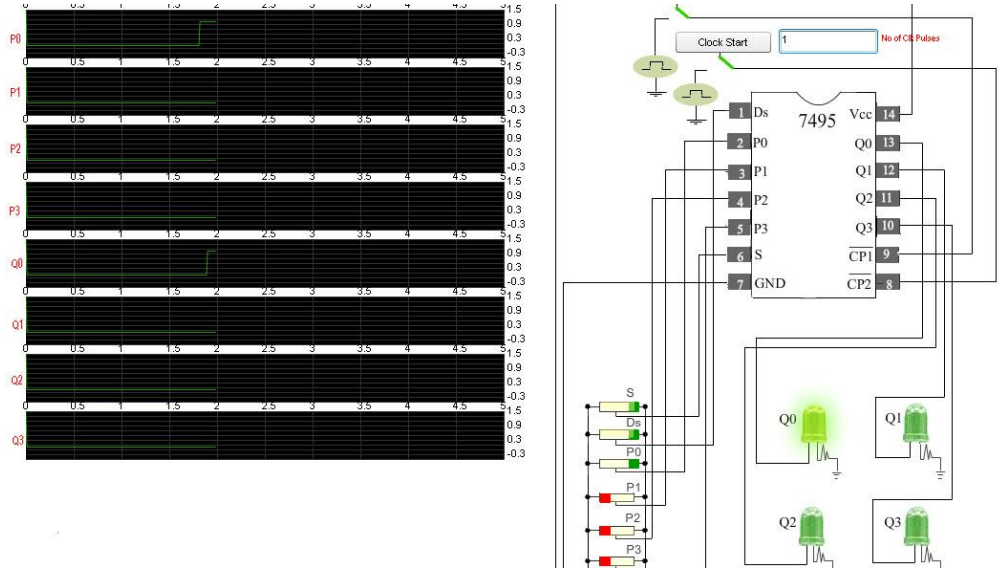
7. Apply high voltage to the mode control input (s).Now the "Clock Start" button for the second clock pulse(CP2) is enabled.Parallel inputs P_0, P_1, P_2, P_3 are enabled.These parallel inputs are directly loaded to the outputs Q_0, Q_1, Q_2, Q_3 respectively.



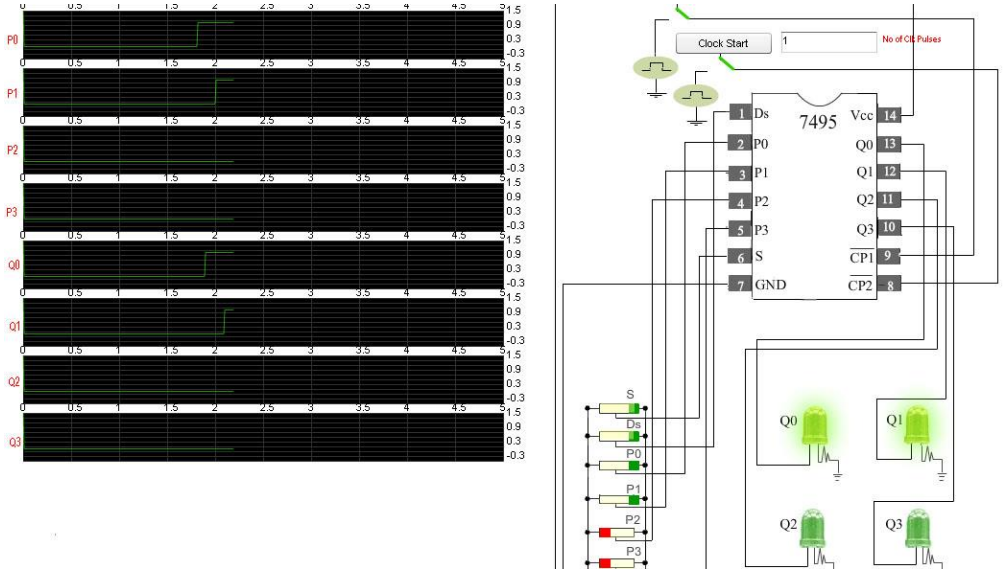
8. Start the clock pulse (CP2).After generation of some clock pulses stop the clock by clicking in "Clock Stop" button.



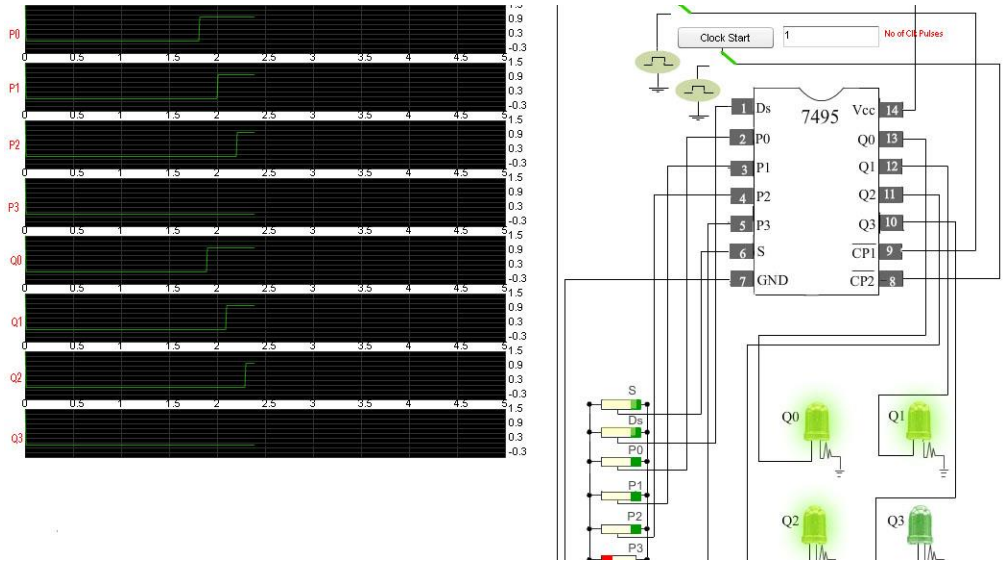
9. Now apply high voltage to P_0 input and set no of clock pulses to 1.See P_0 input is directly loaded to the output Q_0.



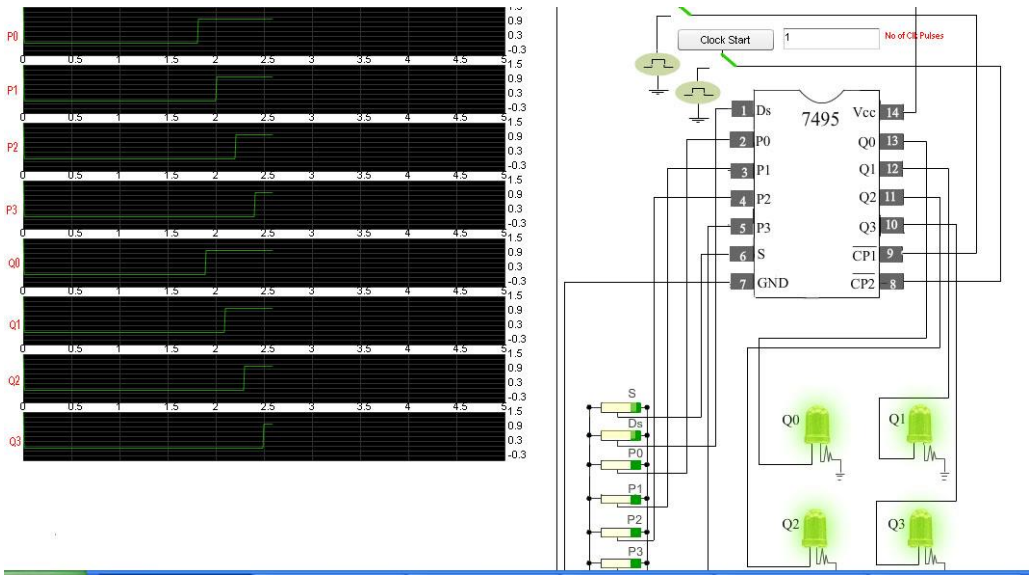
10. Next, apply high voltage to P_1 and start the clock pulse.P_1 input is directly loaded to Q_1.



11. Next, apply high voltage to P_2 and start the clock pulse.P_2 input is directly loaded to Q_2.



12. Now apply high voltage to P_3 and start the clock pulse.P_3 input is directly loaded to Q_3.



Url: https://dec-iitkgp.vlabs.ac.in/exp/multi-bit-sequential-circuits/

Conclusion:

The experiment shows that multi-bit sequential circuits can be successfully analyzed and synthesized using shift registers.

The shift registers correctly store and transfer data across clock pulses, confirming their effectiveness in sequential circuit design.

VIRTUAL LAB -6

Analysis and Synthesis of Logic Functions using Multiplexers

Aim of the experiment:

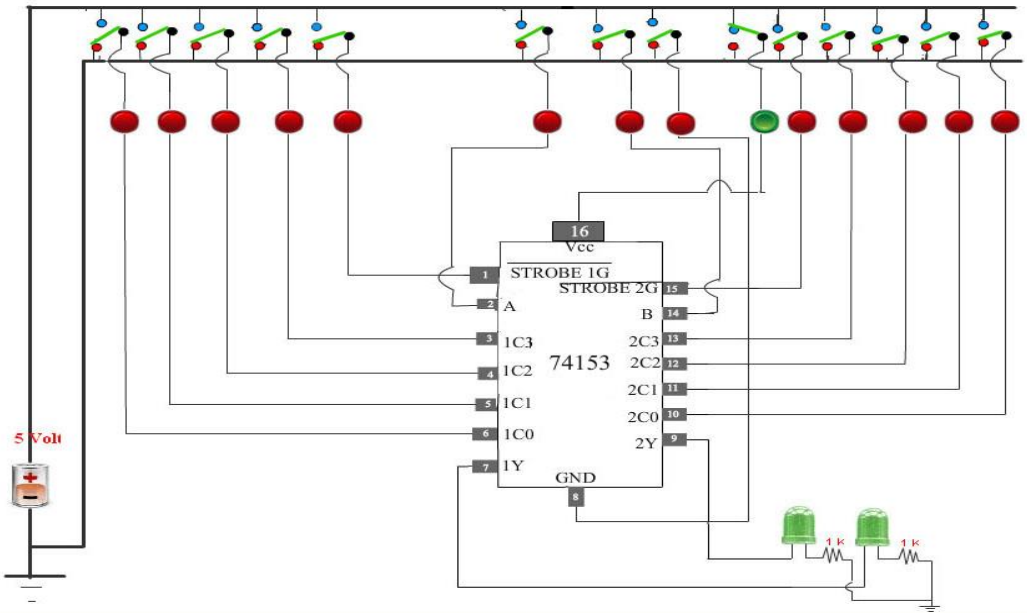
- The principal objective of this experiment(Part 1) is to fully understand the functionality of a Dual 4 line to 1 line Multiplexer(IC 74153) and to show the multiplex function of 74153 in terms of select lines. Note that each of the on-chip multiplexers act independently from the other, while sharing the same select lines
- The principal objective of this experiment(Part 2) is to fully understand the functionality of a Quad 2 line to 1 line Multiplexer(IC 74157) and to show the multiplex function of 74157 in terms of select line. Note that each of the on-chip multiplexers act independently from the other, while sharing the same select line.

Procedure:

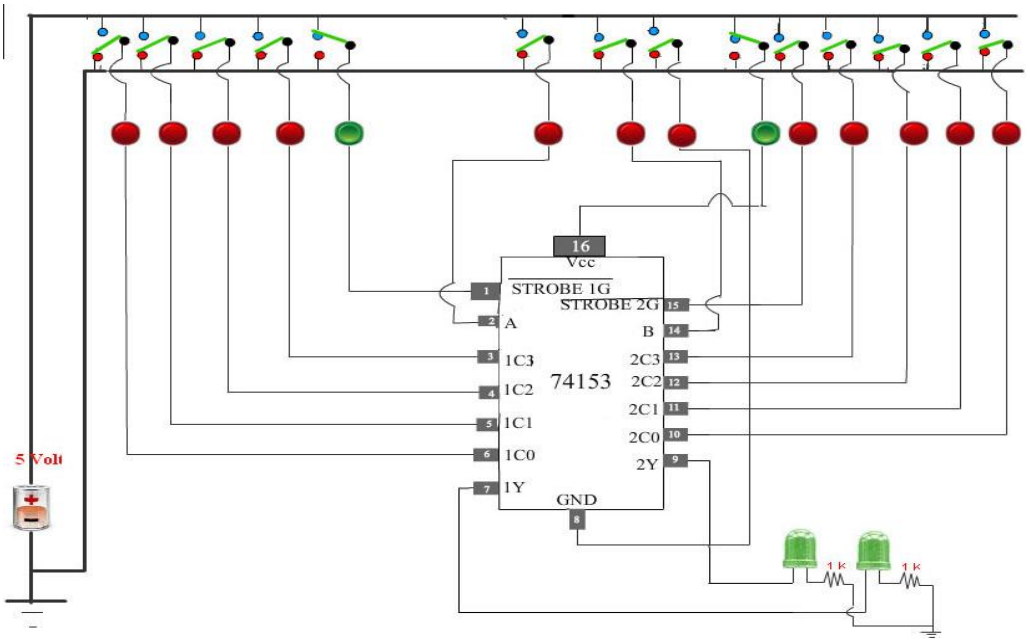
Please follow these steps to do the experiment.

Part 1:

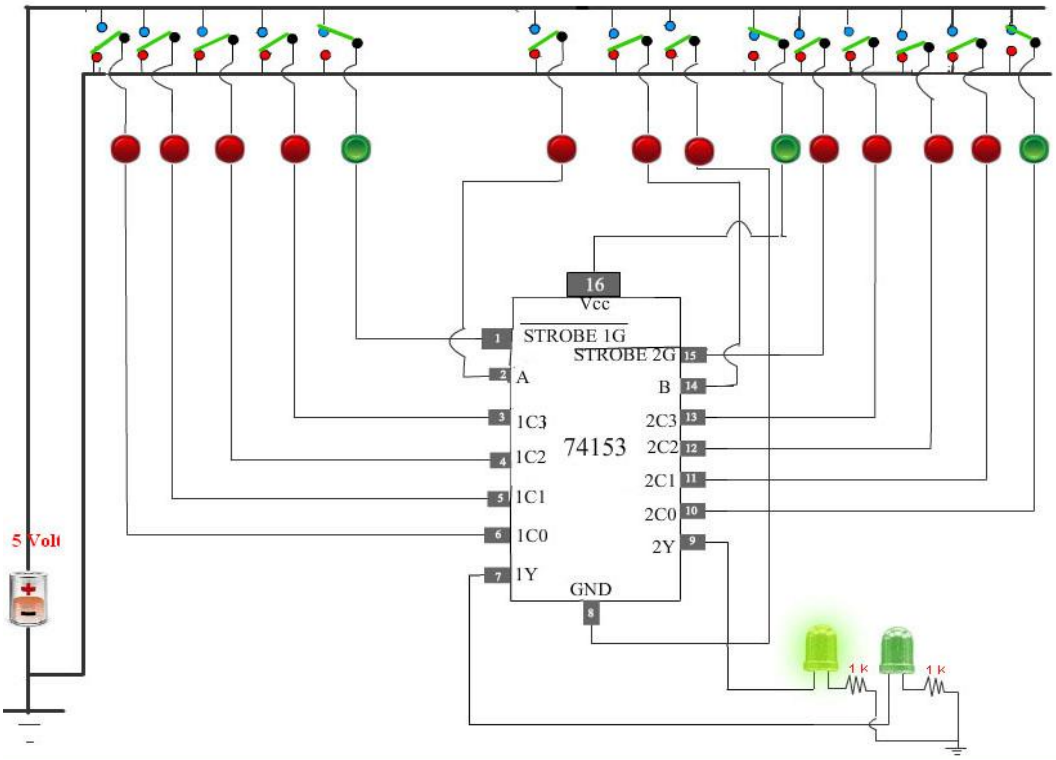
1. At first go through the structure of 74153.Then apply high level voltage to Vcc and low level voltage to GND. If Vcc and ground are not connected properly then error message will be shown and no output will be generated.



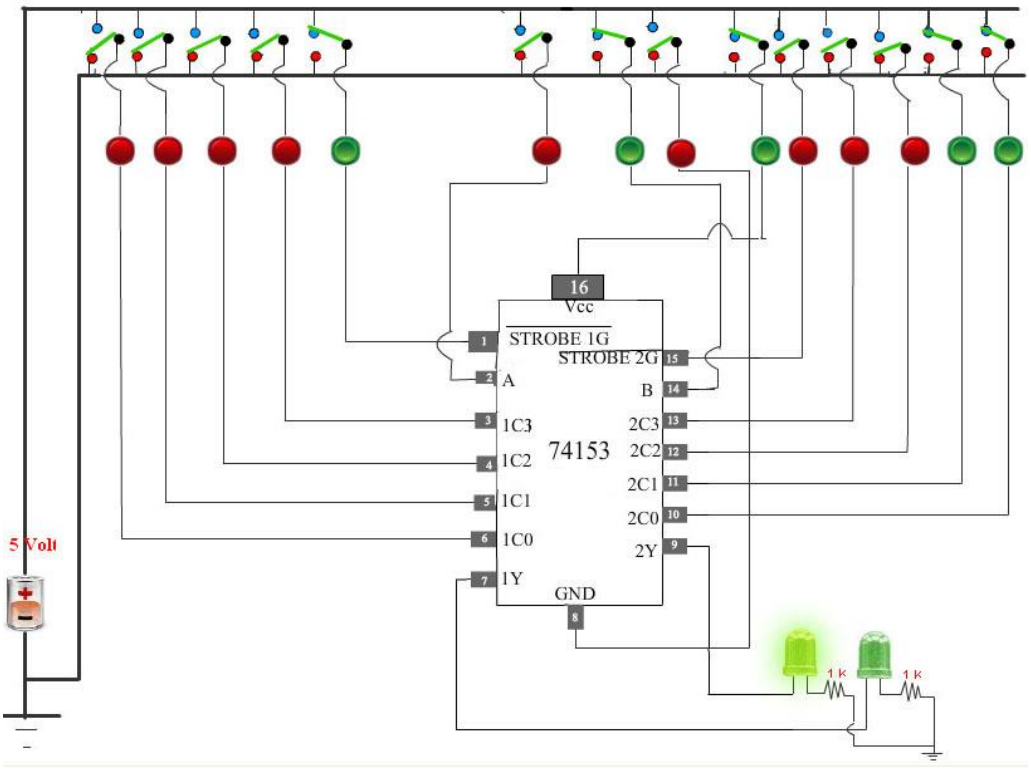
2. Next, apply high level voltage to Strobe1G or strobe 2G. If STROBE 1G is high 2nd Multiplexer is activated . If STROBE 2G is high then 1st Multiplexer is activated.



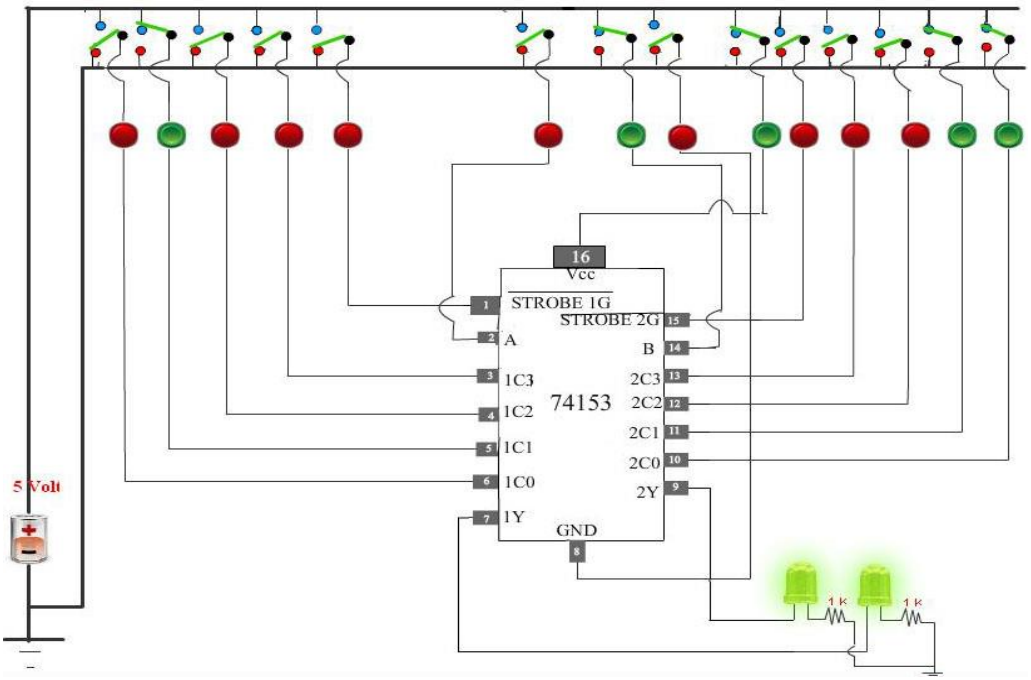
3. Next, apply low level voltage to the select inputs A and B (A Most significant Bit,B Less significant bit). Then apply a high level voltage to 2C0. Now check that how Dual 4 Line to 1 Line Multiplexer select the particular input to be multiplexed and to be applied to the output IY{1 = 1, 2}.



4. For all the combinations of the select inputs A,B verify that both the LEDs are glowing or not glowing. If the LED glows, it indicates that the corresponding output has reached logic 1 level. Similarly a dark LED indicates low level output voltage.

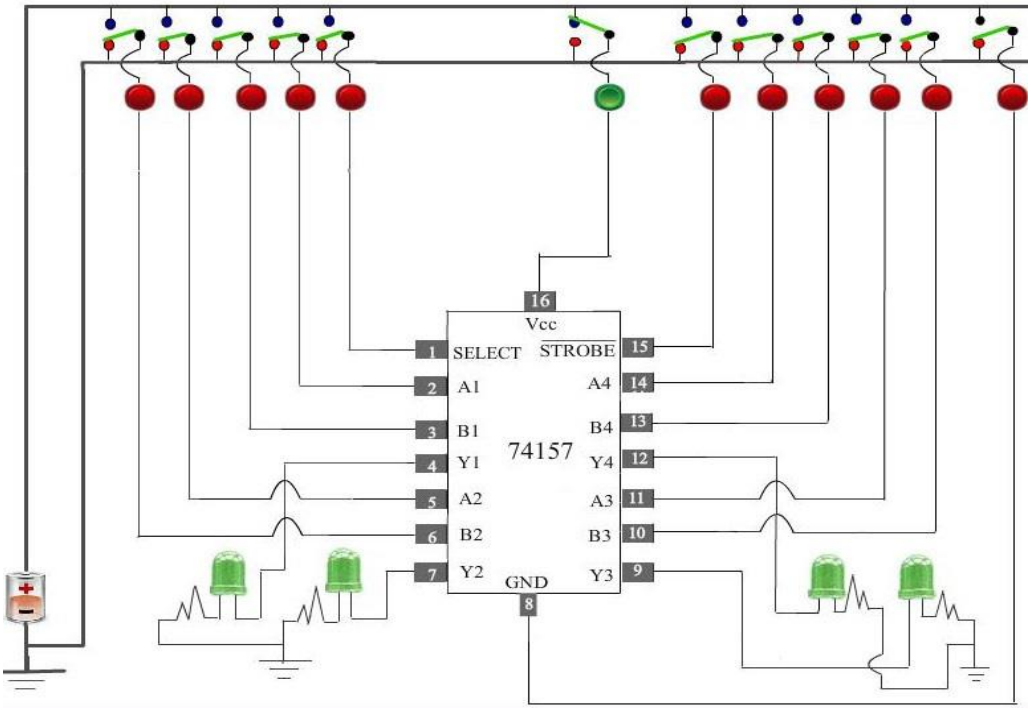


5. If both the Strobe inputs are low then both Multiplexers are activated.

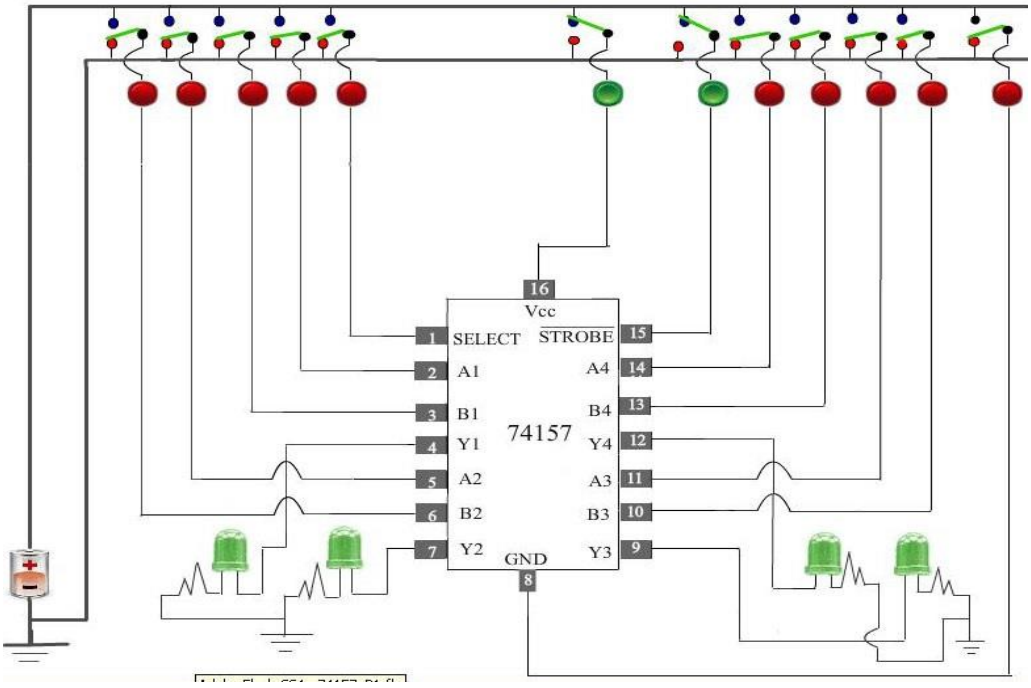


Part 2:

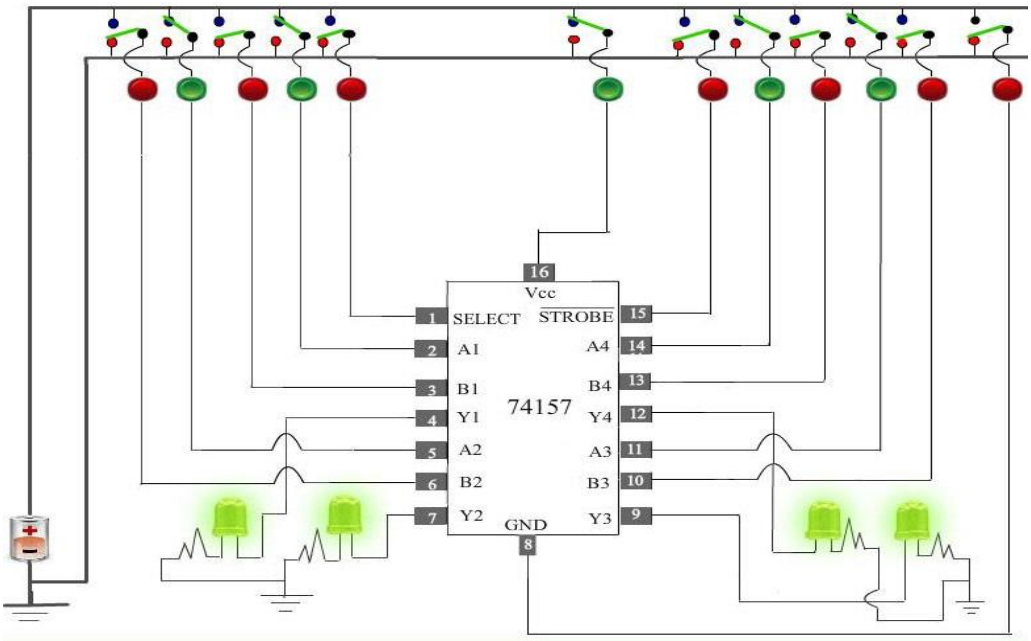
1. At first go through the structure of 74157.Then apply high level voltage to Vcc and low level voltage to GND. If Vcc and ground are not connected properly then error message will be shown and no output will be generated.



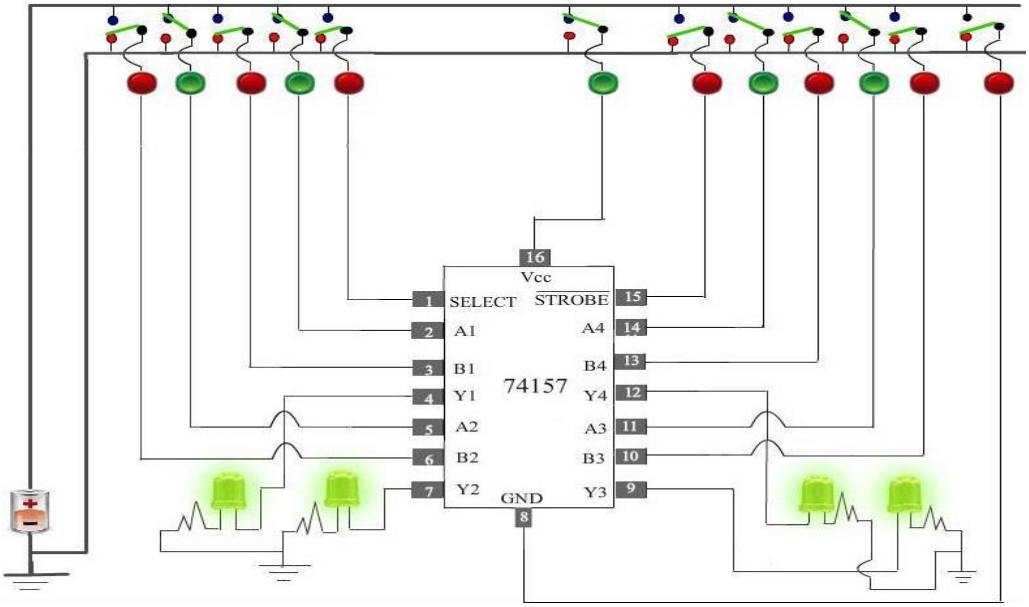
2. Next, apply high level voltage to Strobe input.Now check that all the LEDs are not glowing.Soall the outputs are at low state



3. Next, apply low level voltage to the Strobe input and also apply low level voltage to the Select input. Then apply high level voltage to A1,A2,A3,A4.Now check that all the LEDs are glowing.Because inputs are properly multiplexed to the outputs of the four multiplexers according to the voltage applied to the select input.



4. Next, apply low level voltage to the Strobe input and apply high level voltage to the Select input. Then apply high level voltage to B1,B2,B3,B4. Now check that all the LEDs are glowing.Because inputs are properly multiplexed to the outputs of the four multiplexers according to the voltage applied to the select input.



5. If the LED glows, it indicates that the corresponding output has reached logic 1 level. Similarly a dark LED indicates low level output voltage.

Url: https://dec-iitkgp.vlabs.ac.in/exp/functions-using-multiplexers/index.html

Conclusion:

The experiment demonstrates that complex logic functions can be efficiently implemented using multiplexers.The synthesized circuit produces the correct output for all input combinations, validating the use of multiplexers in logic function realization.

VIRTUAL LAB -7

Analysis and Synthesis of Boolean Relations using Digital Comparators

Aim of the Experiment:

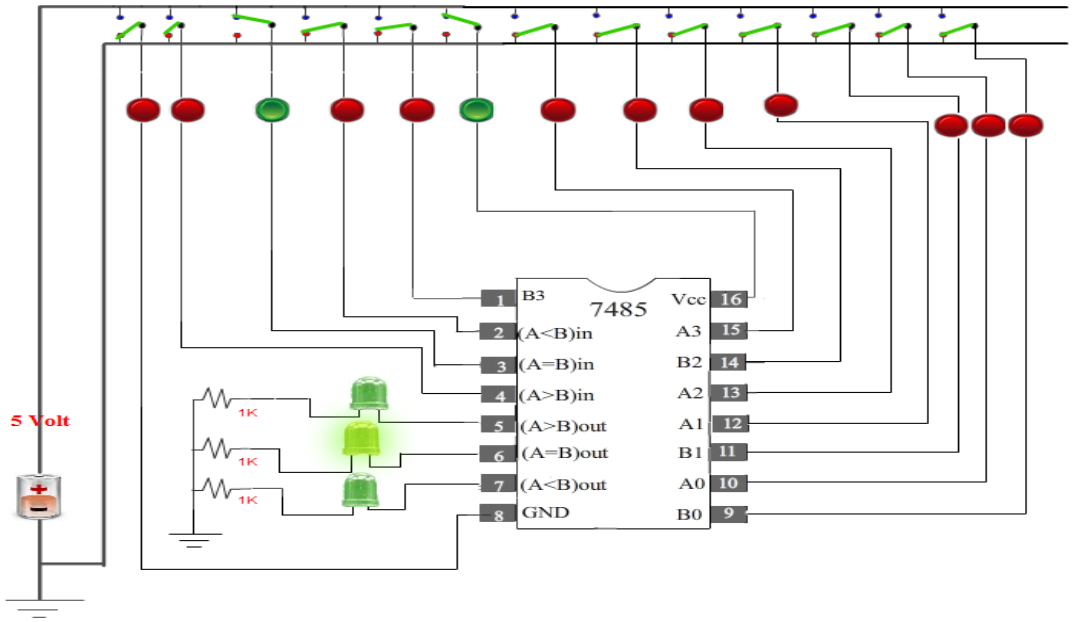
- The objective of Part 1 of the experiment is to fully understand the functionality of 4 bit magnitude comparator using 7485 IC and to show how the comparator output changes according to input combinations of two 4 bit binary numbers.
- The objective of Part 2 of the experiment is to understand the functionality of 8bit magnitude comparator by cascading two four bit magnitude comparator

Procedure:

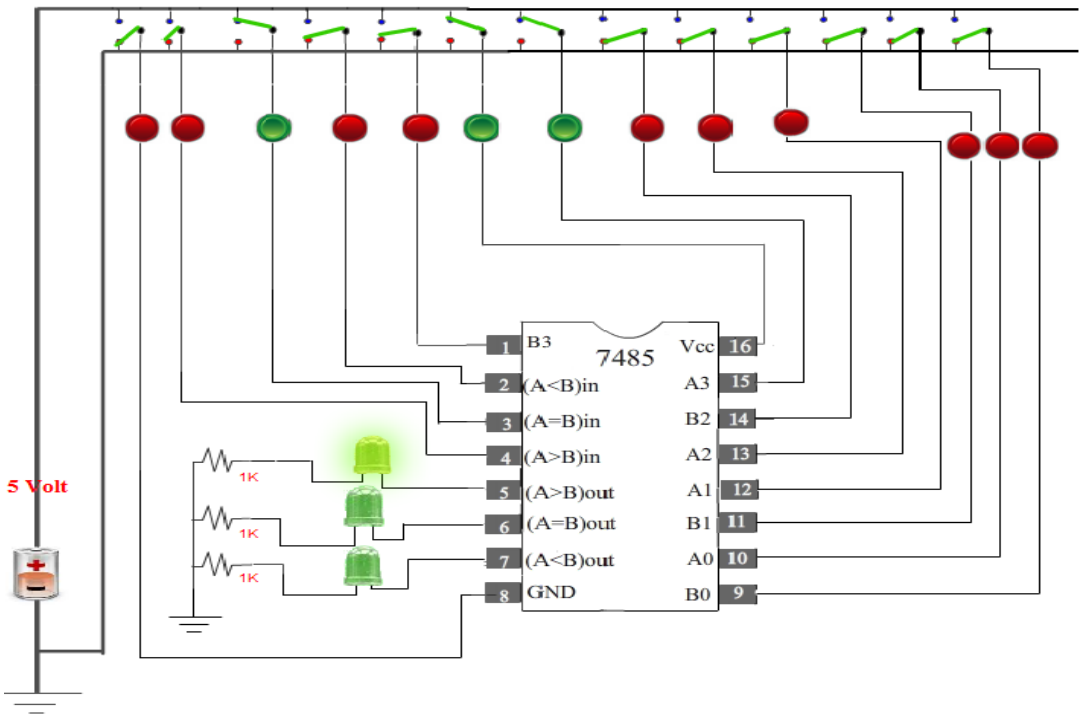
Please follow these steps to do the experiment:

NOTE :

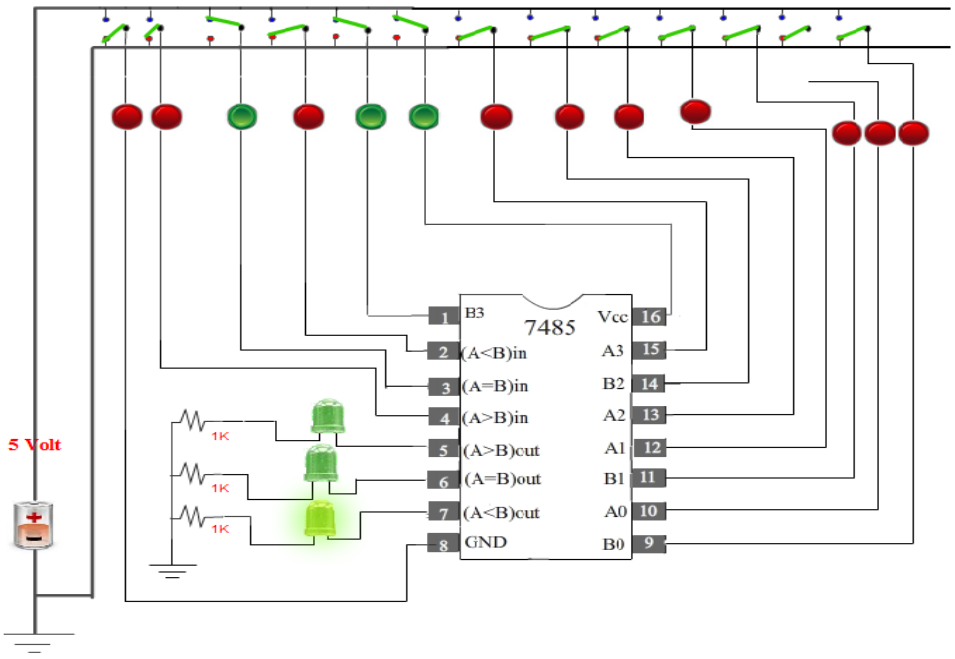
To perform this experiment,it is compulsary always to keep V_{cc} ON, GND OFF, $(A = B)_{IN}$ High, $(A < B)_{IN}$ Low and
$(A > B)_{IN}$ Low.



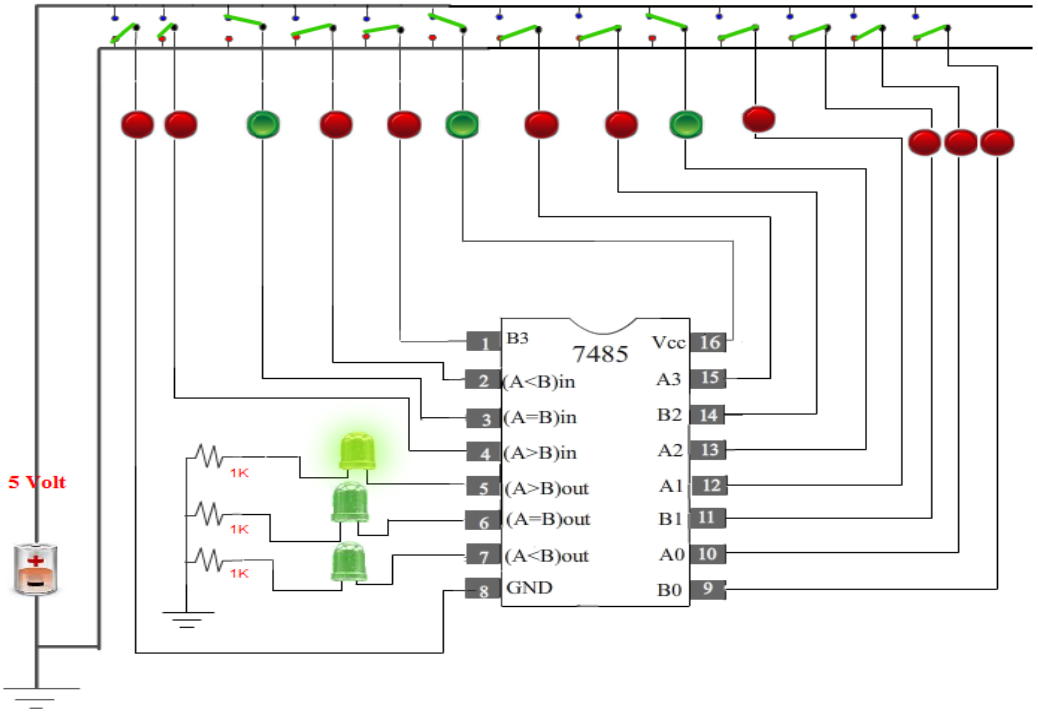
1. At first go through the structure of 7485.Then apply high level voltage to A3 and low level voltage to B3.



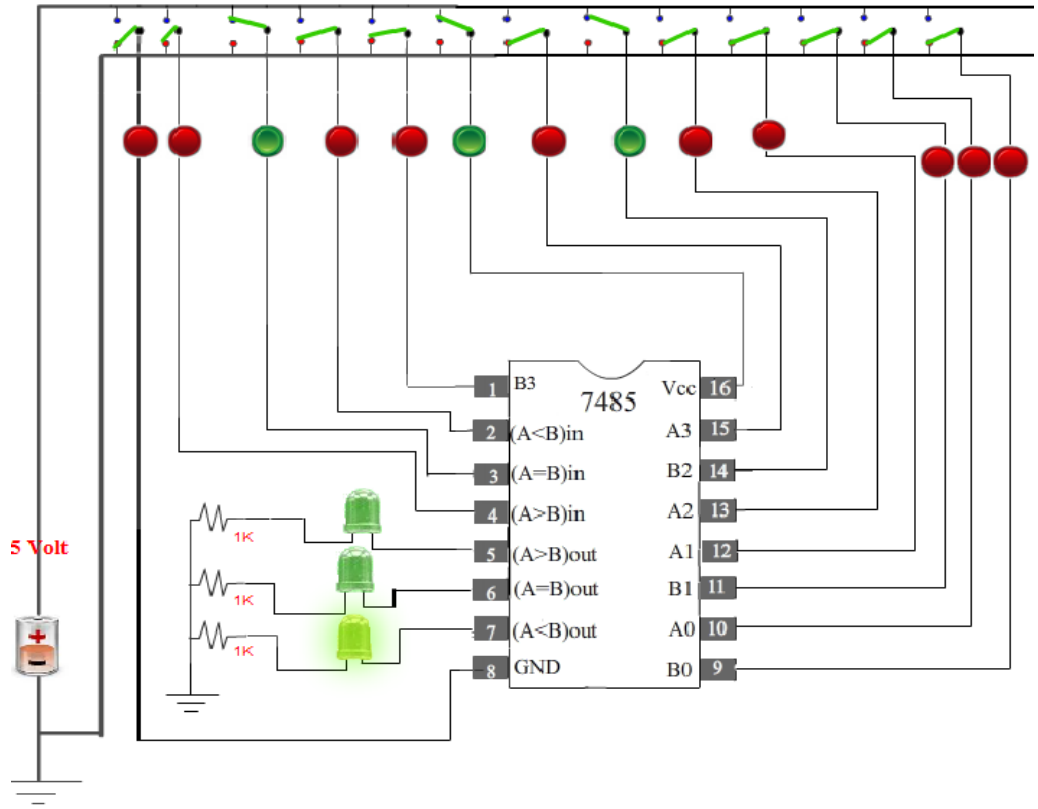
2. Next, apply high level voltage to B3 and low level voltage to A3.



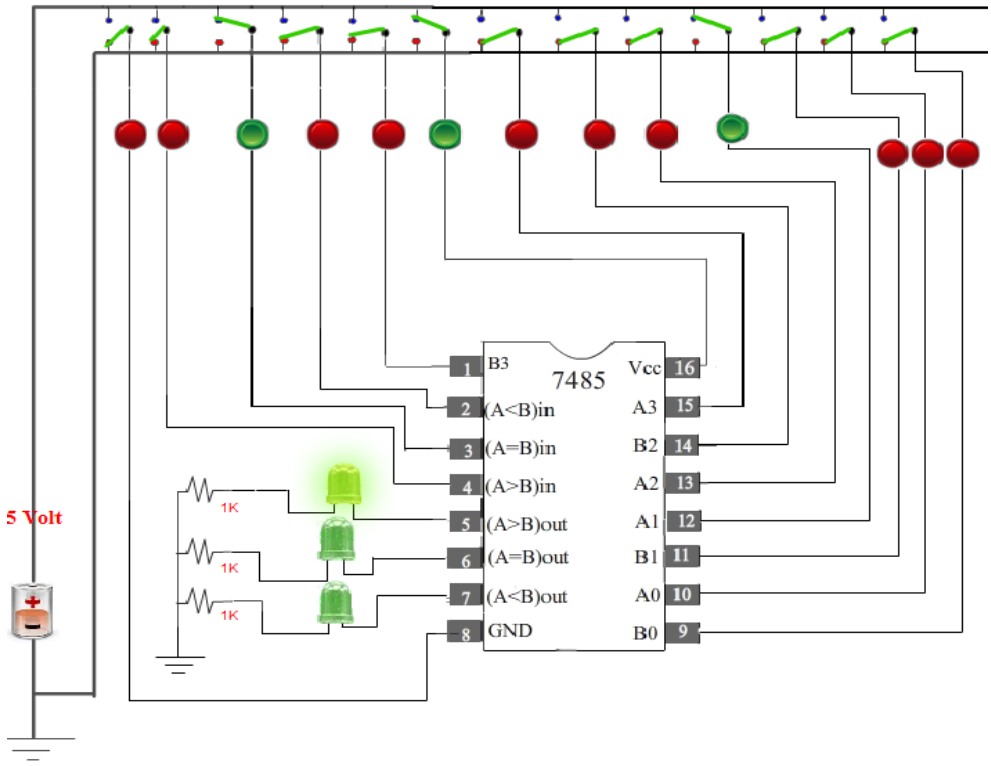
3. Next, apply high level voltage to A2 and low level voltage to B2 and keep same voltage level to A3 & B3 (Either High or Low)



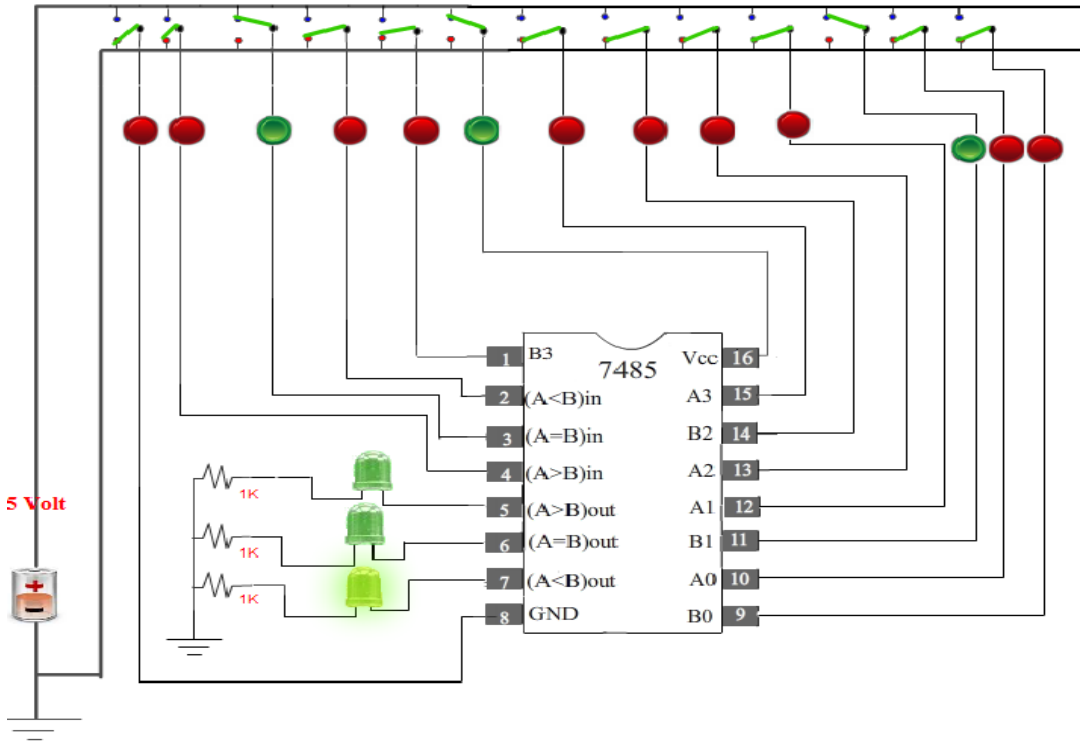
4. Next, apply high level voltage to B2 and low level voltage to A2 and keep same voltage level to A3 & B3 (Either High or Low)



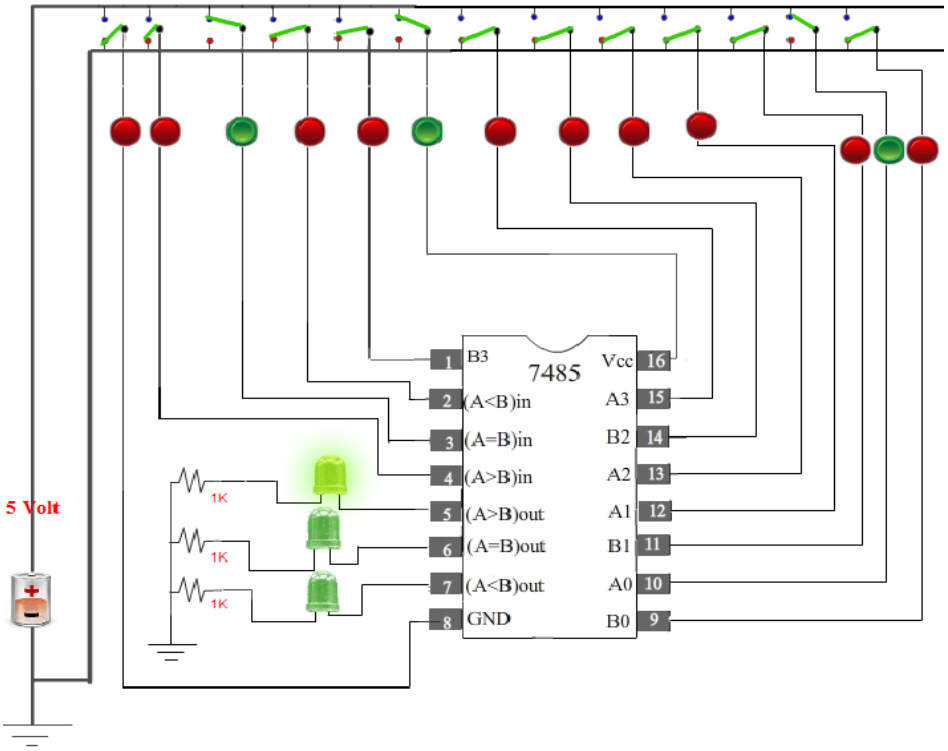
5. Next, apply high level voltage to A1 and low level voltage to B1 and keep same voltage level to A3, B3, A2 and B2 (Either High or Low)



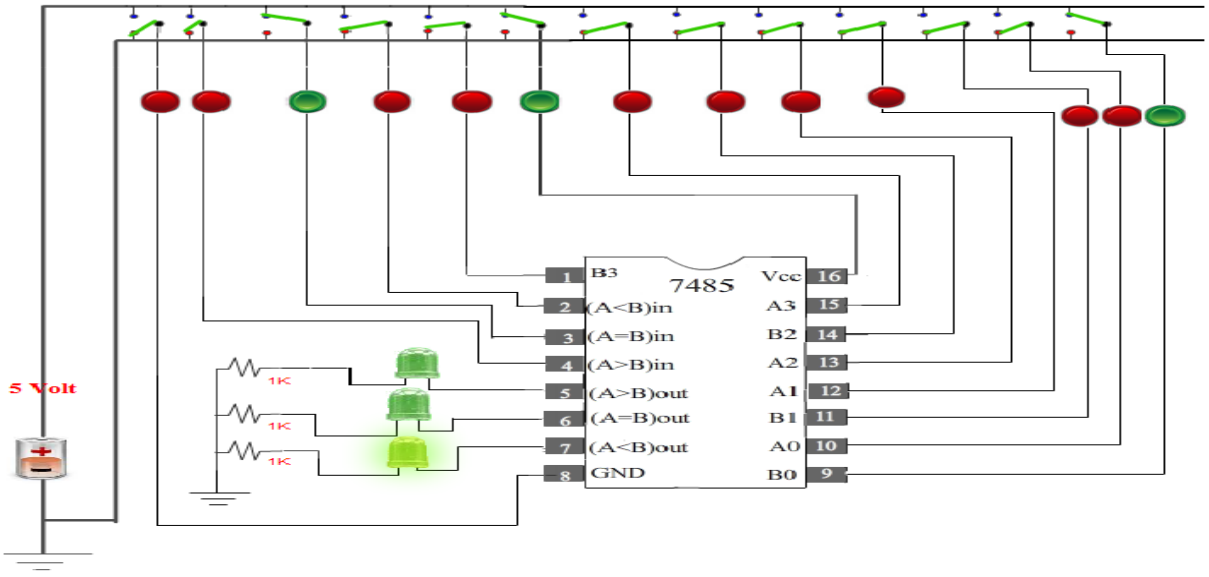
6. ext, apply high level voltage to B1 and low level voltage to A1 and keep same voltage level to A3, B3, A2 and B2 (Either High or Low)



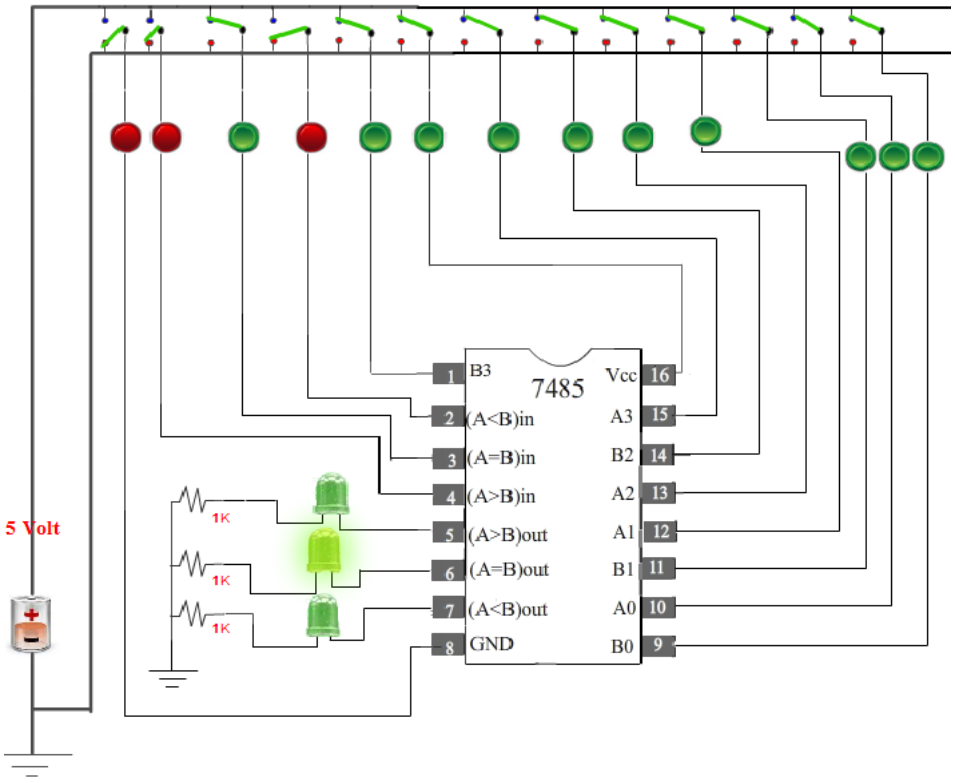
7. Next, apply high level voltage to A0 and low level voltage to B0 and keep same voltage level to A3, B3, A2, B2 A1 and B1 (Either High or Low)



8. Next, apply high level voltage to B0 and low level voltage to A0 and keep same voltage level to A3, B3, A2, B2, A1 and B1 (Either High or Low)



9. ext, apply Same level voltage to A0, B0, A3, B3, A2, B2, A1 and B1 (Either High or Low)



Url: **https://dec-iitkgp.vlabs.ac.in/exp/digital-comparators/**

Conclusion:

The experiment verifies that digital comparators can be used to analyze and synthesize Boolean relations between binary numbers.

The comparator accurately indicates equality, greater-than, and less-than conditions, confirming correct operation.

OPEN ENDED EXPERIMENTS:

1. Mathematical operations using Op-Amp

Aim of the experiment:

To study the following mathematical operations using Operational Amplifier

(a) Addition
(b) Subtraction
(c) Multiplication/division by a constant

Procedure:

Mathematical operations using Op-Amp.

Familiarise with components

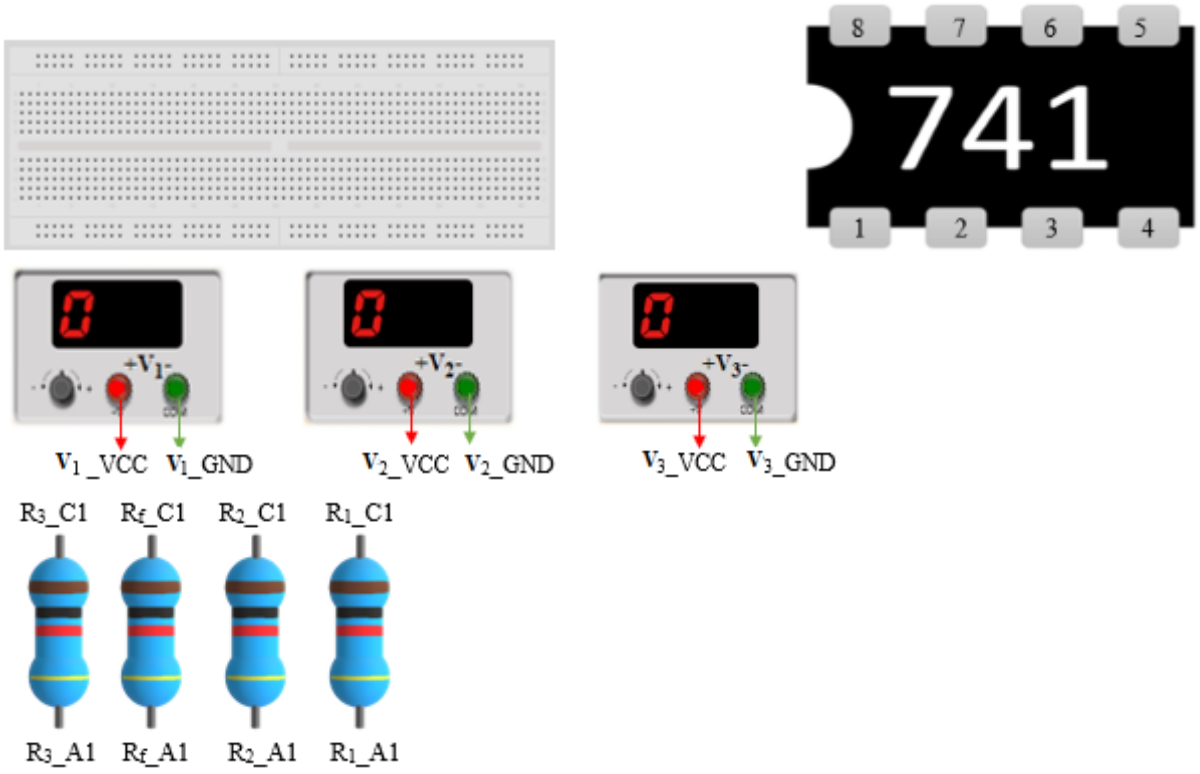


Figure 1: Components

A. Addition

1. Click on the components button to place the component on the table.
2. Make connections as per the circuit diagram or connection table.

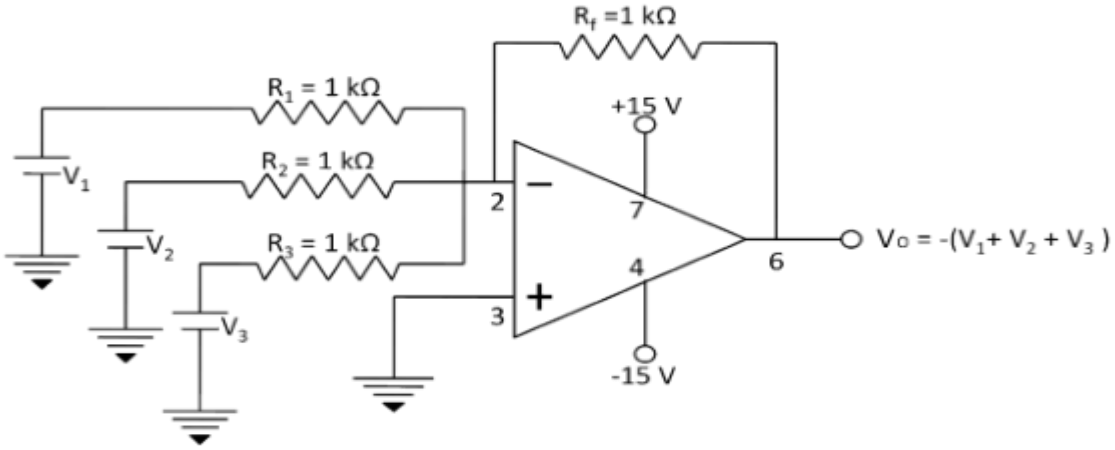


Figure 2: Circuit diagram for addtion.

Table 1: Connection table for addtion.

S. No.	Source	Target
1	IC741_ pin 07	Supply VCC
2	Multimeter_GND	Supply GND
3	IC741_ pin 04	Supply VEE
4	IC741_ pin 03	Supply GND
5	IC741_ pin 06	Multimeter_VCC
6	Power (V_3) _GND	Supply GND
7	Power (V_2) _GND	Supply GND
8	Power (V_1) _GND	Supply GND
9	IC741_ pin 02	Resistance (R_1) _terminal C1
10	Power (V_1) _VCC	Resistance (R_1) _terminal A1
11	IC741_ pin 02	Resistance (R_2) _terminal C1
12	Power (V_2) _VCC	Resistance (R_2) _terminal A1
13	IC741_ pin 02	Resistance (R_3) _terminal C1
14	Power (V_3) _VCC	Resistance (R_3) _terminal A1
15	IC741_ pin 02	Resistance (R_f)_terminal C1
16	IC741_ pin 06	Resistance (R_f)_terminal A1

3. Click on '**Add to table**' button and calculate the output voltage using the formula mentioned in the figure/instructions of respective simulator to add calculations to the table.

B. Subtraction

1. Click on the components button to place the component on the table.
2. Make connections as per the circuit diagram or connection table.

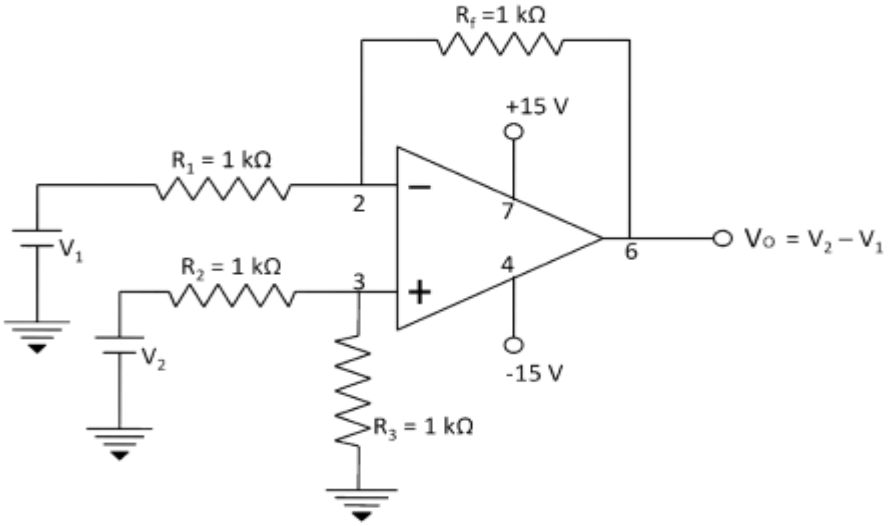


Figure 3: Circuit diagram for subtraction.

Table 2: Connection table for subtraction.

S. No.	Source	Target
1	IC741_ pin 07	Supply VCC
2	Multimeter_GND	Supply GND
3	IC741_ pin 04	Supply VEE
4	IC741_ pin 06	Multimeter_VCC
5	Power (V_2) _GND	Supply GND
6	Power (V_1) _GND	Supply GND
7	IC741_ pin 02	Resistance (R_1) _terminal C1
8	Power (V_1) _VCC	Resistance (R_1) _terminal A1
9	IC741_ pin 03	Resistance (R_2) _terminal C1
10	Power (V_2) _VCC	Resistance (R_2) _terminal A1
11	IC741_ pin 03	Resistance (R_3) _terminal C1
12	Supply GND	Resistance (R_3) _terminal A1
13	IC741_ pin 02	Resistance (R_f)_terminal C1
14	IC741_ pin 06	Resistance (R_f)_terminal A1

3. Click on '**Add to table**' button and calculate the output voltage using the formula mentioned in the figure/instructions of respective simulator to add calculations to the table.

C. Multiplication by constant (and Division when Rf < Ri)

1. Click on the components button to place the component on the table.

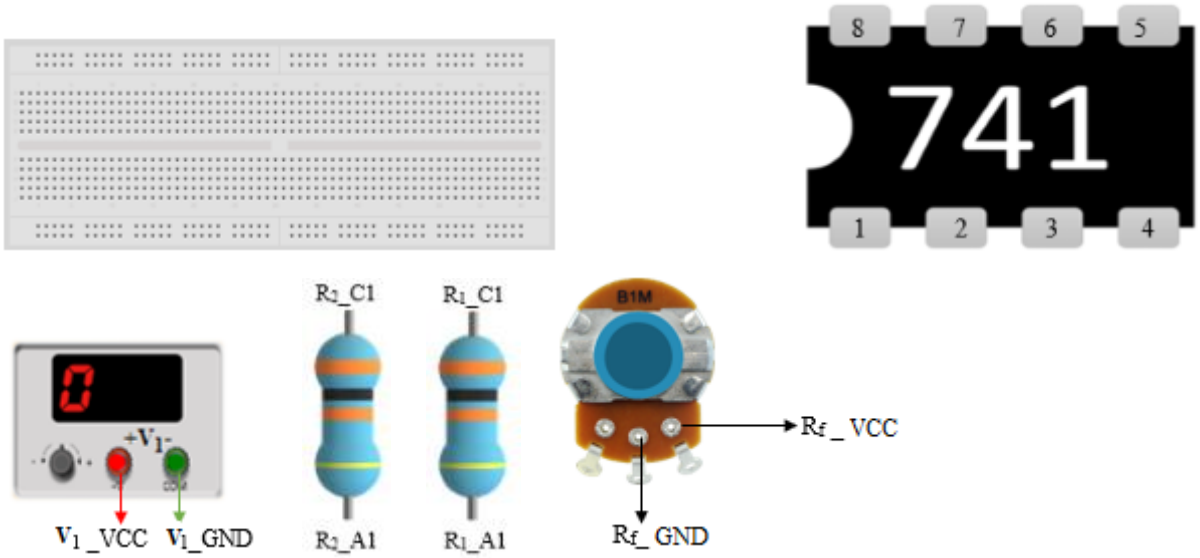


Figure 4: Components

2. Make connections as per the circuit diagram or connection table.

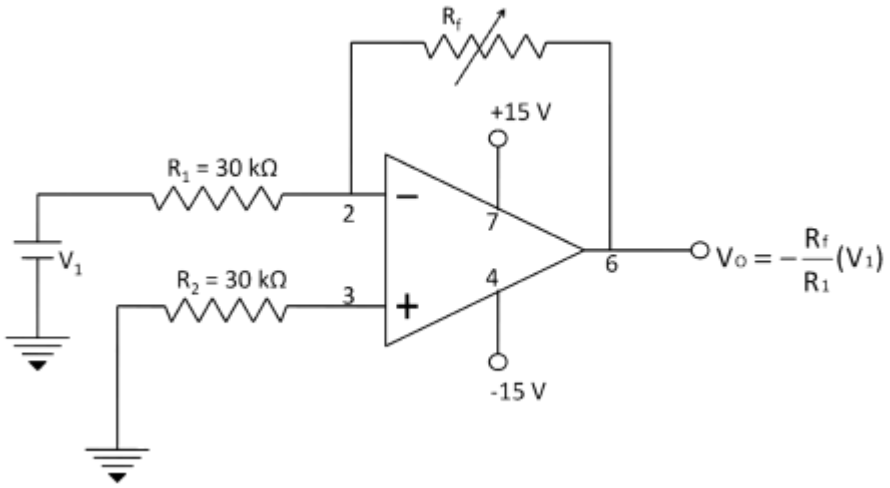


Figure 5: Circuit diagram for multiplication/division by a constant.

Table 3: Connection table for multiplication/division by a constant.

S. No.	Source	Target
1	IC741_ pin 07	Supply VCC
2	Multimeter_GND	Supply GND
3	IC741_ pin 04	Supply VEE
4	IC741_ pin 06	Multimeter_VCC
5	Power (V_1) _GND	Supply GND
6	IC741_ pin 02	Resistance (R_1) _terminal C1
7	Power (V_1) _VCC	Resistance (R_1) _terminal A1
8	IC741_ pin 03	Resistance (R_2) _terminal C1
9	Supply GND	Resistance (R_2) _terminal A1
10	IC741_ pin 02	Resistance (R_f) _VCC
11	IC741_ pin 06	Resistance (R_f) _GND

3. Click on '**Add to table**' button and calculate the output voltage using the formula mentioned in the figure/instructions of respective simulator to add calculations to the table.

Url: https://ade2-iitr.vlabs.ac.in/exp/mathematical-operations/index.html

Conclusion:

The operational amplifier is successfully used to perform mathematical operations such as addition, subtraction, integration, and differentiation.
The observed outputs closely match theoretical values, confirming the accuracy and versatility of op-amps in analog computation.

2. To verify De-Morgan's Theorems

Aim of the experiment:

To verify De-Morgan's theorems.

Procedure:

1. Under Simulation, click Theorem 1 or Theorem 2.

Familiarise with components

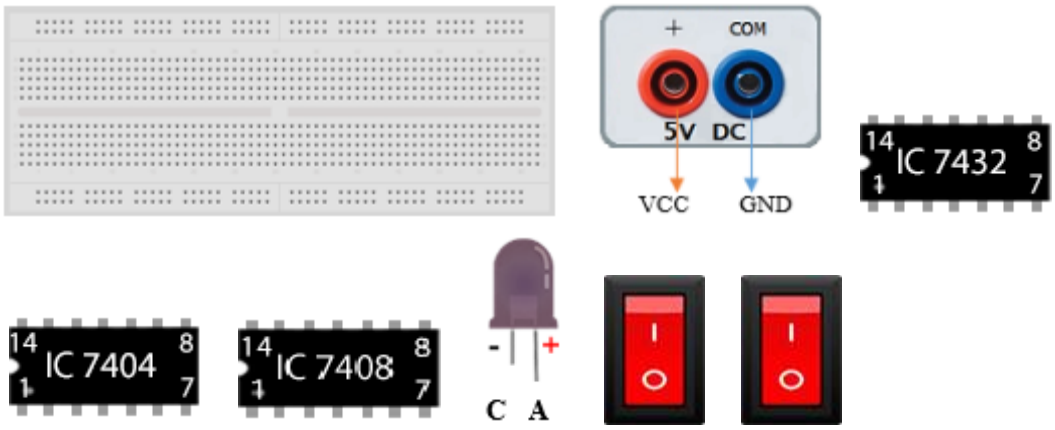


Figure 1: Components

1st Theorem :-

L.H.S. term for De-Morgan's 1st theorem, i.e (A + B)' :–

1. Click on the Component button to place components on the table.
2. Make connections as per the circuit diagram and pin diagrams of ICs or according to connection table.

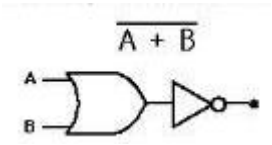


Figure 2 Circuit diagram of (A + B)'

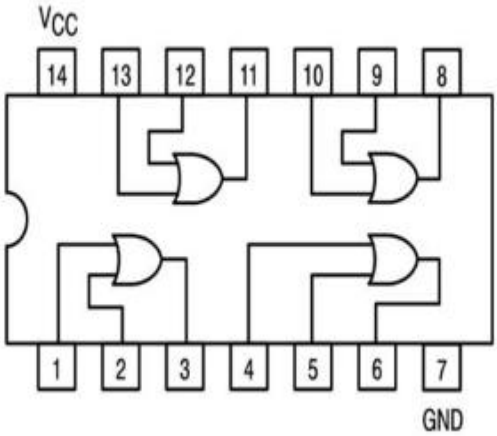


Figure 3 Pin diagram of IC 7432

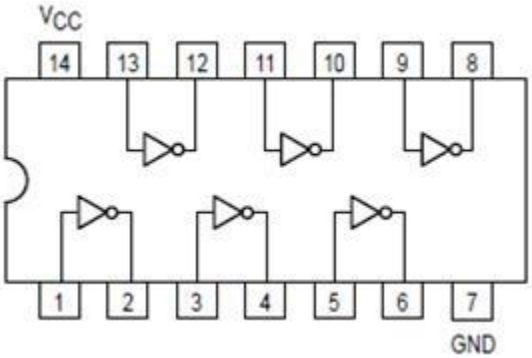


Figure 4 Pin diagram of IC 7404

Table 1: Connection table for (A + B)'

S. No.	Source	Target
1	IC7432 _ Pin 14	Supply VCC
2	IC7432 _ Pin 07	Supply GND
3	IC7404 _ Pin 14	Supply VCC
4	IC7404 _ Pin 07	Supply GND
5	Led _ terminal C	Supply GND
6	Switch _ terminal A	IC7432 _ Pin 13
7	Switch _ terminal B	IC7432 _ Pin 12
8	IC7432 _ Pin 11	IC7404 _ Pin 13
9	IC7404 _ Pin 12	Led _ terminal A

3. Click on Check Connections button. If connections are right, click on 'OK', then Simulation will become active.
4. Provide the input by clicking toggle switches A and B.
5. Fill the observed values in the Truth Table.
6. Verify Truth Table by clicking on Check button, if outputs are correct then click on OK.
7. Click on the Result button provided below the table.

R.H.S. term for De-Morgan's 1st theorem, i.e A'B' :–

1. Click on the Component button to place components on the table.
2. Make connections as per the circuit diagram and pin diagrams of ICs or according to connection table.

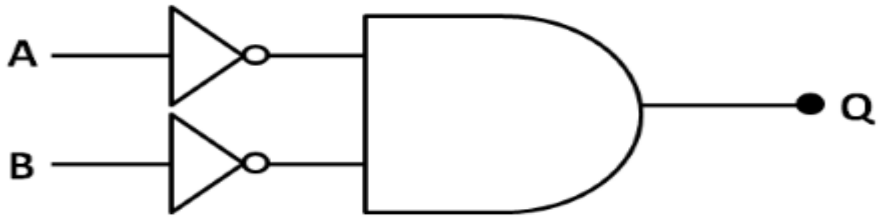


Figure 5: Circuit diagram of A'.B'

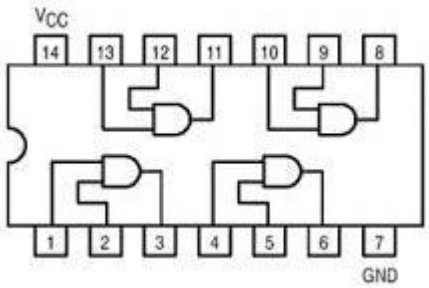


Figure 6: Pin diagram of IC 7408

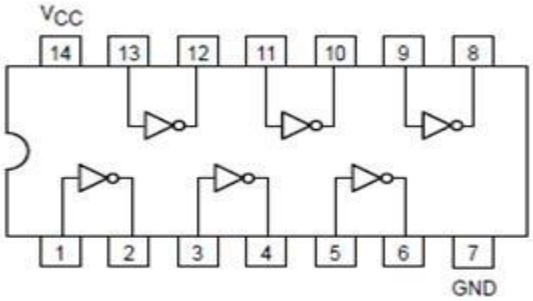


Figure 7 Pin diagram of IC 7404

Table 2: Connection table for A'.B'

S. No.	Source	Target
1	IC7404 _ Pin 14	Supply VCC
2	IC7404 _ Pin 07	Supply GND
3	IC7408 _ Pin 14	Supply VCC
4	IC7408 _ Pin 07	Supply GND
5	Led _ terminal C	Supply GND
6	Switch _ terminal A	IC7404 _ Pin 13
7	Switch _ terminal B	IC7404 _ Pin 11
8	IC7404 _ Pin 12	IC7408 _ Pin 13
9	IC7404 _ Pin 10	IC7408 _ Pin 12
10	IC7408 _ Pin 11	Led _ terminal A

3. Click on Check Connections button. If connections are right, click on 'OK', then Simulation will become active.
4. Provide the input by clicking toggle switches A and B.
5. Fill the observed values in the Truth Table.
6. Verify Truth Table by clicking on Check button, if outputs are correct then click on OK.
7. Click on the Result button provided below the table.

2nd Theorem :-

L.H.S. term for De-Morgan's 2nd theorem, i.e (A.B)' :–

1. Click on the Component button to place components on the table.
2. Make connections as per the circuit diagram and pin diagrams of ICs or according to connection table.

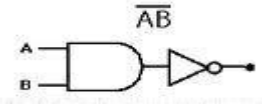


Figure 8: Circuit diagram of (A.B)'

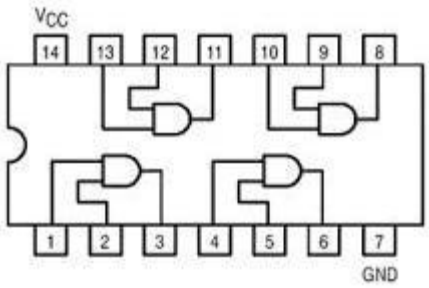
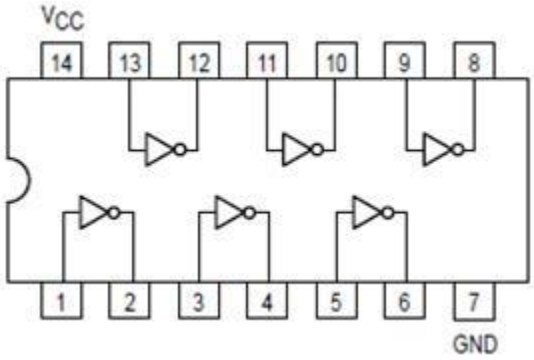


Figure 9: Pin diagram of IC 7408



Figue 10: Pin diagram of IC 7404

Table 3: Connection table for (A.B)'

S. No.	Source	Target
1	IC7408 _ Pin 14	Supply VCC
2	IC7408 _ Pin 07	Supply GND
3	IC7404 _ Pin 14	Supply VCC
4	IC7404 _ Pin 07	Supply GND
5	Led _ terminal C	Supply GND
6	Switch _ terminal A	IC7408 _ Pin 13
7	Switch _ terminal B	IC7408 _ Pin 12
8	IC7408 _ Pin 11	IC7404 _ Pin 13
9	IC7404 _ Pin 12	Led _ terminal A

3. Click on Check Connections button. If connections are right, click on 'OK', then Simulation will become active.
4. Provide the input by clicking toggle switches A and B.
5. Fill the observed values in the Truth Table.
6. Verify Truth Table by clicking on Check button, if outputs are correct then click on OK.
7. Click on the Result button provided below the table.

R.H.S. term for De-Morgan's 2nd theorem, i.e (A' + B') :–

1. Click on the Component button to place components on the table.
2. Make connections as per the circuit diagram and pin diagrams of ICs or according to connection table.

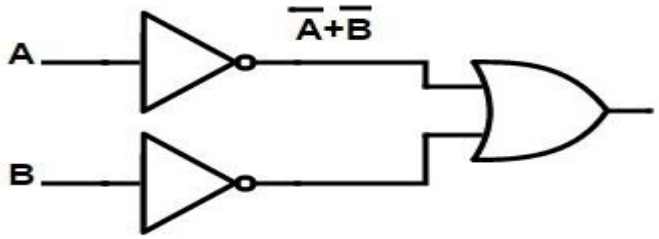


Figure 11: Circuit diagram of (A' + B')

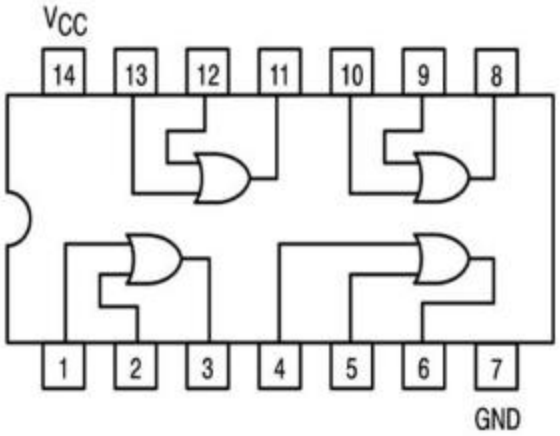


Figure 12: Pin diagram of IC 7432

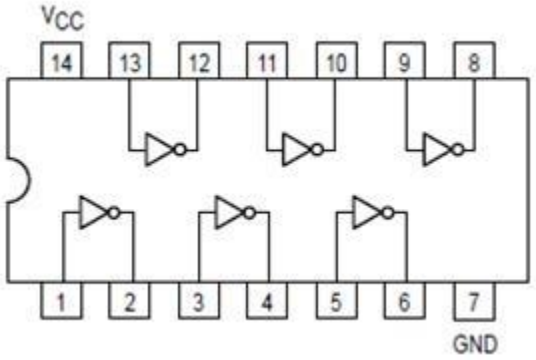


Figure 13: Pin diagram of IC 7404

Table 4: Connection table for (A' + B')

S. No.	Source	Target
1	IC7404 _ Pin 14	Supply VCC
2	IC7404 _ Pin 07	Supply GND
3	IC7432 _ Pin 14	Supply VCC
4	IC7432 _ Pin 07	Supply GND
5	Led _ terminal C	Supply GND
6	Switch _ terminal A	IC7404 _ Pin 13
7	Switch _ terminal B	IC7404 _ Pin 11
8	IC7404_ Pin 12	IC7432 _ Pin 13
9	IC7404_ Pin 10	IC7432 _ Pin 12
10	IC7432 _ Pin 11	Led _ terminal A

3. Click on Check Connections button. If connections are right, click on 'OK', then Simulation will become active.
4. Provide the input by clicking toggle switches A and B.
5. Fill the observed values in the Truth Table.
6. Verify Truth Table by clicking on Check button, if outputs are correct then click on OK.
7. Click on the Result button provided below the table.

Url: **https://ade-iitr.vlabs.ac.in/exp/de-morgans-theorems/**

Conclusion:

The experiment verifies De Morgan's theorems by showing the equivalence between complemented sums and products.

Thus, logical expressions can be simplified and implemented using alternative gate configurations with the same functionality.

3. Even/Odd Parity Generator

Aim of the experiment:

To design a 3-bit even/odd parity generator circuit.

Procedure:

Click on either the "Even Parity Generator" or "Odd Parity Generator" option from the "Simulation" tab.

Familiarise with components:

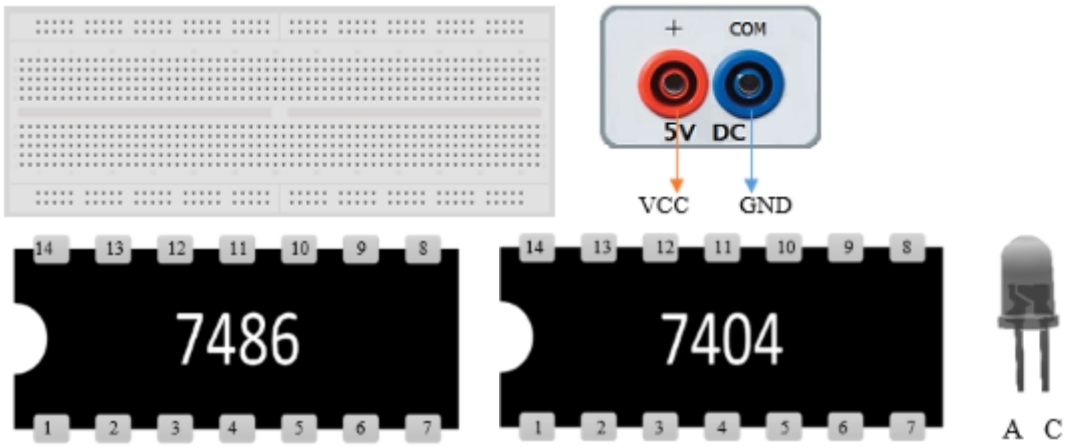


Figure 1: Components

Follow these steps to perform the experiment on simulator:

A. Even Parity Generator:

1. Fill the truth table and click on 'CHECK' button.
2. Click on the component button to place the component on the table.
3. Make connections as per the circuit diagram and pin diagram of the IC or according to connection table.

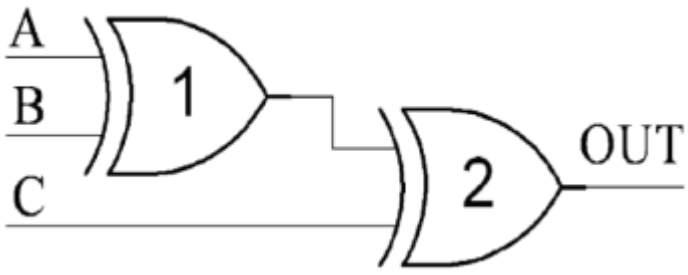


Figure 2: Circuit diagram of even parity generator.

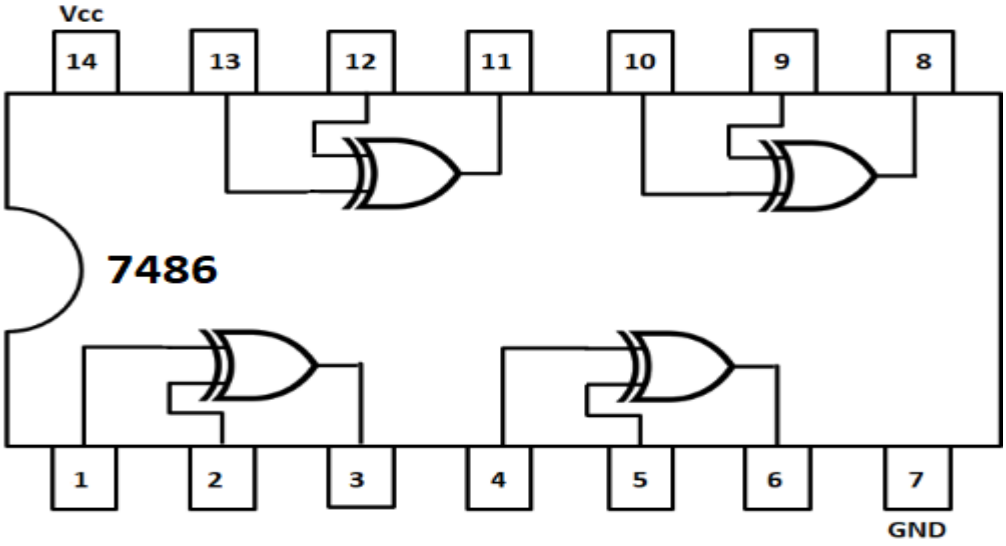


Figure 3: Pin diagram of IC-7486.

4. Feed input A and B to one gate of IC and input C to another gate.
5. Click on 'Check Connections' button. If connections are right, the 'Start Simulation' button will become active. Click on it to start simulation.
6. Click on the toggle switches 'A', 'B' and 'C' to perform simulation.

B. Odd Parity Generator:

1. Fill the truth table and click on 'CHECK' button.
2. Click on the component button to place the component on the table.
3. Make connections as per the circuit diagram and pin diagrams of the ICs or according to connection table.

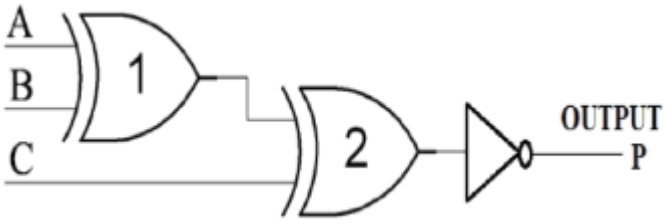


Figure 4: Circuit diagram of odd parity generator.

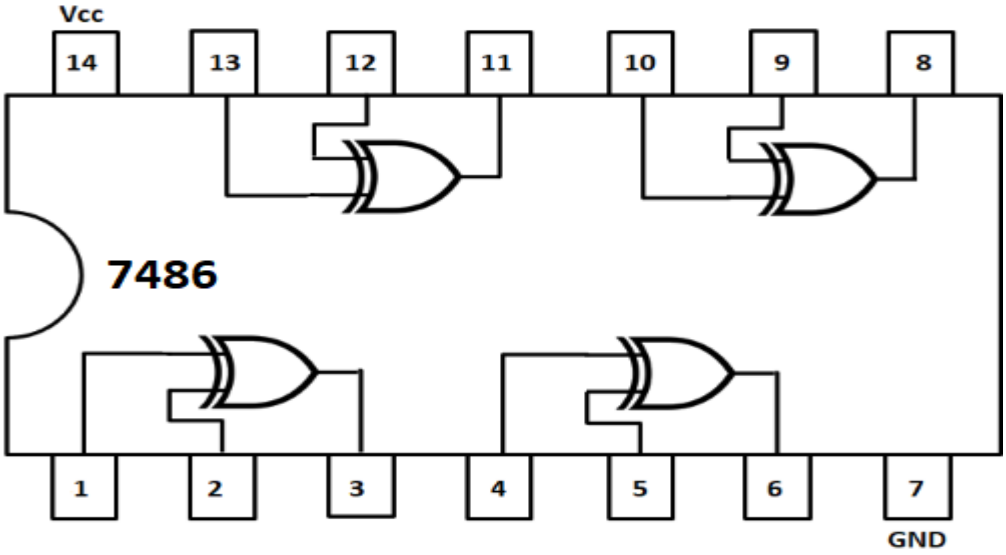


Figure 5: Pin diagram of IC-7486.

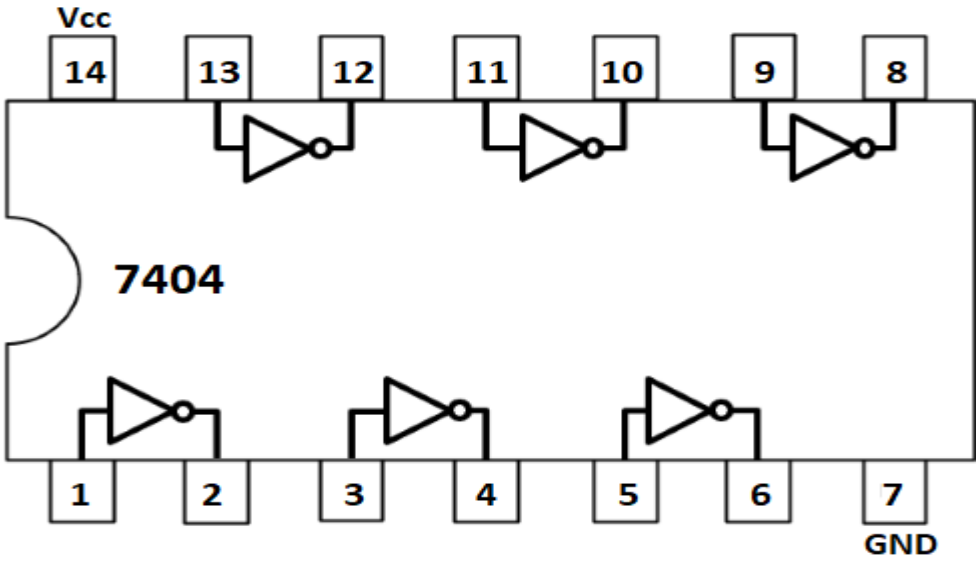


Figure 6: Pin diagram of IC-7404.

Table : Connection table for odd parity generator

S. No.	Source	Target
1	IC7486_ Pin 14	Supply VCC
2	IC7486_ Pin 07	Supply GND
3	IC7404_ Pin 14	Supply VCC
4	IC7404_ Pin 07	Supply GND
5	Led _ terminal C	Supply GND
6	Input _terminal A	IC7486_ Pin 01
7	IC7486_ Pin 02	Input _terminal B
8	IC7486_ Pin 03	IC7486_ Pin 04
9	IC7486_ Pin 05	Input _terminal C
10	IC7486_ Pin 06	IC7404_ Pin 01
11	Led _ terminal A	IC7404_ Pin 02

4. Feed input A and B to one gate of IC and input C to another gate.
5. Click on 'Check Connections' button. If connections are right, the 'Start Simulation' button will become active. Click on it to start simulation.
6. Click on the toggle switches 'A', 'B' and 'C' to perform simulation.

Url: **https://ade-iitr.vlabs.ac.in/exp/parity-generator/**

Conclusion:

The even and odd parity generator circuits were designed and verified successfully.

The outputs correctly indicate parity for all input combinations, confirming reliable error detection capability.