MARRI LAXMAN REDDY
INSTITUTE OF TECHNOLOGY AND MANAGEMENT
(AN AUTONOMOUS INSTITUTION)
(Approved by AICTE, New Delhi & Affiliated to JNTUH, Hyderabad)
Accredited by NBA and NAAC with 'A' Grade & Recognized Under Section2(f) & 12(B)of the UGC act,1956

INTEGRATED CIRCUITS APPLICATIONS LABORATORY MANUAL

III YEAR I SEMESTER

REGULATION: MLRS R24

AY:2026-2027

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINNERING

COURSE STRUCTURE, OBJECTIVES & OUTCOMES

COURSE STRUCTURE

Level	Credits	Periods/week	Prerequisites
UG	1	3	-

Evaluation Scheme:

MID (Internal Lab) Semester Test	30 marks
Day to day evaluation	10 marks
End Semester Lab external Examination	60 marks

The end semester examination shall be conducted with an external examiner and internal examiner.

The external examiner shall be appointed by the principal / Chief Controller of examinations.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION

LINEAR AND DIGITAL IC APPLICATIONS

LABORATORY MANUAL

Virtual lab details

Name of the Virtual Lab: NA
Virtual Lab Host Institute: NA
URL/Link to Lab: NA
Academic Year: NA
Semester: NA

CERTIFICATE

This is to certify that this manual is a bonafide record of practical work in the

Integrated Circuits Applications Laboratory in Vth Semester of III -year B. Tech Sem I (ECE) Programme during the academic year 2023-2024. This book is prepared by Mrs. P.Lavanya (Assistant Professor) Department of Electronics and Communication Engineering.

LAB I/C **Head of the Department**

PREFACE

Integrated Circuits (ICs) are essential building blocks in the world of electronics, each contributing to the functionality of modern devices in unique ways. Linear ICs, which process continuous signals, are primarily used in applications that require precise amplification, regulation, and analog signal processing. These include audio equipment, sensors, power management systems, and other scenarios where signal fidelity and smooth operation are critical. By maintaining a direct, proportional relationship between input and output, Linear ICs are vital in ensuring that real-world analog signals, such as sound or temperature, are accurately captured and controlled in electronic systems.

Digital ICs, on the other hand, operate with discrete signals and are the foundation of digital processing, computation, and control. They power microprocessors, memory chips, and logic circuits, enabling devices like computers, smartphones, and automated systems to perform complex tasks. Digital ICs are built on binary systems, where signals exist in two distinct states, '0' and '1', allowing for rapid processing, data storage, and decision-making. Together, Linear and Digital ICs enable the seamless integration of analog and digital systems, driving innovations across a wide range of industries, from consumer electronics to industrial automation and communications.

By,

Mrs. P.Lavanya

ACKNOWLEDGEMENT

It was really a good experience, working with Integrated Circuits Applications Laboratory. First, we would like to thank **Dr. N. Srinivas**, Assoc. Professor, HOD of Department of Electronics and Communication Engineering, Marri Laxman Reddy Institute of technology & Management for his concern and giving the technical support in preparing the document.

We are deeply indebted and gratefully acknowledge the constant support and valuable patronage of **Dr. Ravi Prasad**, Dean, Marri Laxman Reddy Institute of technology & Management for giving us this wonderful opportunity for preparing the Analog and Digital Communications Laboratory manual.

We express our hearty thanks to **Dr.R.Murali Prasad**, Principal, Marri Laxman Reddy Institute of technology & Management, for timely corrections and scholarly guidance.

At last, but not the least I would like to thanks the entire ECE Department faculty those who had inspired and helped us to achieve our goal.

By,

Mrs. P.Lavanya

GENERAL INSTRUCTIONS

1. Students should report to the concerned labs as per the timetable schedule.

2. Students who turn up late to the labs will in no case be permitted to perform the experiment scheduled for the day.

3. After completion of the experiment, certification of the concerned staff in-charge in the observation book is necessary.

4. Students should bring a notebook of about 100 pages and should enter the readings/observations into the notebook while performing the experiment.

5. The record of observations along with the detailed experimental procedure of the experiment.

6. Performed in the immediate last session should be submitted and certified by the staff member in-charge.

7.. Not more than one student is permitted to perform the experiment on a setup.

8. When the experiment is completed, students should disconnect the setup made by them, and should return all the components/instruments taken for the purpose.

9. Any damage of the equipment or burnout of components will be viewed seriously by putting penalty.

10. Students should be present in the labs for the total scheduled duration.

11. Students are required to prepare thoroughly to perform the experiment before coming to Laboratory.

12. Procedure sheets/data sheets provided to the student's should be maintained neatly and to be returned after the experiment.

SAFETY PRECAUTIONS

1. No horseplay or running is allowed in the labs.

2. No bare feet or open sandals are permitted.

3. Before energizing any equipment, check whether anyone is in a position to be injured by your actions.

4. Read the appropriate equipment instruction manual sections or consult with your instructor.

5. Before applying power or connecting unfamiliar equipment or instruments into any circuits.

6. Position all equipment on benches in a safe and stable manner.

7. Do not make circuit connections by hand while circuits are energized. This is especially.

8. Dangerous with high voltage and current circuits.

INSTITUTE VISION AND MISSION

Vision of the Institute

To be a globally recognized institution that fosters innovation, excellence, and leadership in education, research, and technology development, empowering students to create sustainable solutions for the advancement of society.

Mission of the Institute

To foster a transformative learning environment that empowers students to excel in engineering, innovation, and leadership.

To produce skilled, ethical, and socially responsible engineers who contribute to sustainable technological advancements and address global challenges.

To shape future leaders through cutting-edge research, industry collaboration, and community engagement.

Quality Policy

The management is committed in assuring quality service to all its stakeholders, students, parents, alumni, employees, employers, and the community. Our commitment and dedication are built into our policy of continual quality improvement by establishing and implementing mechanisms and modalities ensuring accountability at all levels, transparency in procedures, and access to information and actions.

DEPARTMENT VISION AND MISSION

Vision of the Department

To provide quality technical education in Electronics and Communication Engineering through research, innovation, striving for global recognition in specified domain, leadership, and sustainable societal solutions.

Mission of the Department

- **DM1:** To create a transformative learning environment that empowers students in electronics and communication engineering, fostering excellence in technical skills and leadership.
- **DM2:** To drive innovation through research, deliver a transformative education grounded in ethical principles, and nurture the development of professionals
- **DM3:** To cultivate strong industry partnerships, and engaging actively with the community for societal and technological progress.

PROGRAMME EDUCATIONAL OBJECTIVES

PEO 1: Have successful careers in Industry

PEO2: Show Excellence in Higher Studies/ Research

PEO3: Show Good competency towards entrepreneurship.

PROGRAM OUTCOMES (PO):

PO 1: Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and engg. specialization to the solution of complex engineering problems.

PO 2: Problem analysis: Identify, formulate, research literature, and analyze engineering problemsto arrive at substantiated conclusions using first principles of mathematics, natural, and engineering sciences.

PO 3: Design/development of solutions: Design solutions for complex engineering problems and design system components, processes to meet the specifications with consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO 4: Conduct investigations of complex problems: Use research-based knowledge including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO 5: Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO 6: The engineer and society: Apply reasoning informed by the contextual knowledge to assesssocietal, health, safety, legal, and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO 7: Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO 8: Ethics: Apply ethical principles and commit to professional ethics and responsibilities andnorms of the engineering practice.

PO 9: Individual and team work: Function effectively as an individual, and as a member or leaderin teams, and in multidisciplinary settings.

PO 10: Communication: Communicate effectively with the engineering community and with society at large. Be able to comprehend and write effective reports documentation. Make effective presentations, and give and receive clear instructions.

PO 11: Project management and finance: Demonstrate knowledge and understanding of engineering and management principles and apply these to one’s own work, as a member and leader in a team. Manage projects in multidisciplinary environments.

PO 12: Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PROGRAM SPECIFIC OUTCOMES

PSO 1: Analyze and design analog & digital circuits or systems for a given specification and function.

PSO2: Implement functional blocks of hardware-software co-designs for signal processing and communication applications.

PSO 3: Gain the hands-on competency skills in computing tools for electronics and communication systems for the entry level position to meet the employer's requirements

COURSE STRUCTURE:

Level	Credits	Periods/Week	Prerequisites
UG	1	3	Entire subject of Analog and DigitalCommunications.

EVALUATION SCHEME:

MID (Internal Lab) Semester Test	20 Marks
Day to day evaluation	20 Marks
End Semester Lab external Examination	60 Marks

Evaluation Scheme:

Each laboratory will be evaluated for a total of 100 marks consisting of 40 marks for Continuous Internal Evaluation (CIE) and 60 marks for semester end lab examination. Out of 40 marks for internal evaluation:

- A write-up on day-to-day experiment(aim,components/procedure, expected outcome) which shall be evaluated for 10 marks
- 10 marks for viva-voce/ tutorial/ case study/ application/ poster presentation.
- Internal practical examination shall be evaluated for 10 marks.
- The remaining 10 marks are for Laboratory Project (Design/ Software / Hardware Model/ App Development/ Prototype).

Table 1: CIE marks distribution

Component				
Type of Assessment	Day to Day performance and viva voce examination	Final internal lab assessment	Laboratory Report / Project and Presentation	Total Marks
CIE marks	20	10	10	40

Continuous Internal Evaluation (CIE): Two CIE exams shall be conducted at the 8^{th} week and 16th week of the semester; the average of the two CIEs will be taken into account. The CIE exam is conducted for 10 marks.

The Semester End Examination shall be conducted with an external examiner and the laboratory teacher. The external examiner shall be appointed from the other colleges which will be decided by the Head of the institution.

In the Semester End Examination held for 3 hours, total 60 marks are divided and allocated as shown below:

- 10 marks for write-up
- 15 for experiment/program
- 15 for evaluation of results
- 10 marks for presentation on another experiment/program in the same laboratory course and
- 10 marks for viva-voce on concerned laboratory course.

COURSE OBJECTIVES:

The students will try to learn

- The characteristics of op-amp
- Filter characteristics using IC741
- The operation of IC 555
- Designing of combinational circuits using ICs
- Implementation of the sequential circuits using ICs

COURSE OUTCOMES:

After successful completion of the course, students shall be able to

- Apply IC 741 and IC 555 in Practical Circuit Design
- Design and Implement Timer-Based Circuits Using IC 555
- Implement and Optimize IC 741 Filter Circuits for Signal Conditioning
- Analyze the Performance of Combinational Circuits
- Design sequential Circuits Using Digital ICs

MAPPING OF EACH CO WITH PO(s), PSO(s):

Course Outcomes	PROGRAM OUTCOMES												PSOs		
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2	PSO 3
CO1	✓	✓	✓	-	✓	-	-	-	-	-	-	-	✓	✓	✓
CO2	✓	-	✓	✓	✓	-	-	-	-	-	-	-	✓	✓	✓
CO3	✓	✓	✓	✓	✓	-	-	-	-	-	-	-	✓	-	-
CO4	✓	✓	✓	✓	✓	-	-	-	-	-	-	-	✓	-	-
CO5	✓	-	✓	✓	✓	-	-	-	-	-	-	-	✓	✓	✓

JUSTIFICATIONS FOR CO – PO / PSO MAPPING - DIRECT:

Course Outcomes	PO'S/ PSO'S	Justification for mapping (Students will be able to)	No. of Key Competencies
CO1	PO1	1. Application of scientific principles and methodologies.	1
	PO2	1. Recognizing and defining complex engineering problems or opportunities. 2. Structuring and abstracting the problem for systematic analysis. 3. Examining research literature 4. Investigating problems using data collection and relevant methodologies.	4
	PO3	1. Investigate and define a problem while identifying constraints, including environmental, sustainability, health, and safety considerations. 2. Understand customer and user needs while considering factors such as aesthetics. 3. Identify and manage cost drivers in engineering solutions. 4. Use creativity to develop innovative engineering solutions. 5. Ensure fitness for purpose across production, operation, maintenance, and disposal. 6. Manage the design process and evaluate outcomes for safety and risk assessment.	6

	PO5	1. Develop engineering solutions using modern tools across various disciplines.	`1
	PSO1	1. Analyze response of a circuit or system 2. Design of a circuit or system for a given specification	2
	PSO2	1. Develop Operational block diagrams 2. Proficiency in the use of software tools for circuit design.	2
CO2	PO1	1. Utilization of mathematical concepts in problem-solving. 2. Integration of knowledge from various engineering disciplines.	2
	PO3	1. Understand customer and user needs while considering factors such as aesthetics. 2. Identify and manage cost drivers in engineering solutions. 3. Use creativity to develop innovative engineering solutions. 4. Ensure fitness for purpose across production, operation, maintenance, and disposal.	4
	PO4	1. Develop essential laboratory and workshop skills to carry out experimental investigations and gather reliable data. 2. Address complex problems in various engineering contexts, including operations, management, and technology development. 3. Leverage technical literature and reliable information sources	3
	PO5	Identify appropriate prediction and modeling tools for diverse engineering applications	`1
	PSO1	1. Analyze response of a circuit or system 2. Design of a circuit or system for a given specification 3. Understand and apply circuit or system specifications accurately. 4. Knowledge of analog and digital signal processing techniques.	4

	PSO2	1. Develop Operational block diagrams 2. Proficiency in the use of software tools for circuit design.	2
CO3	PO1	1. . Integration of knowledge from various engineering disciplines.	1
	PO2	1. Recognizing and defining complex engineering problems or opportunities. 2. Structuring and abstracting the problem for systematic analysis. 3. Examining research literature 4. Investigating problems using data collection and relevant methodologies. 5. Applying mathematical, natural, and engineering sciences in problem-solving. 6. Ensuring accuracy and reliability through validation. 7. Planning and conducting experiments for problem analysis. 8. Implementing and testing solutions through experimentation.	8
	PO3	1. Understand customer and user needs while considering factors such as aesthetics. 2. Identify and manage cost drivers in engineering solutions. 3. Use creativity to develop innovative engineering solutions. 4. Ensure fitness for purpose across production, operation, maintenance, and disposal. 5. Manage the design process and evaluate outcomes for safety and risk assessment. 6. Understand the commercial and economic context of engineering processes.	6
	PO4	1. Gain a deep understanding of materials, equipment, processes, and products through research to address engineering problems effectively. 2. Develop essential laboratory and workshop skills to carry out experimental investigations and gather reliable data. 3. Address complex problems in various engineering contexts, including operations,	6

		management, and technology development. 4. Leverage technical literature and reliable information sources 5. Follow appropriate codes of practice and industry standards when analyzing and interpreting experimental data. 6. Ensure high-quality results by integrating various data sources and considering quality control during engineering investigations.	
	PO5	1. Utilize IT tools in engineering analysis, design, and decision-making.	1
	PSO1	1. Analyze response of a circuit or system 2. Design of a circuit or system for a given specification	2
CO4	PO1	1. Integration of knowledge from various engineering disciplines.	1
	PO2	1. Structuring and abstracting the problem for systematic analysis. 2. Examining research literature 3. Investigating problems using data collection and relevant methodologies. 4. Applying mathematical, natural, and engineering sciences in problem-solving. 5. Ensuring accuracy and reliability through validation. 6. Planning and conducting experiments for problem analysis. 7. Implementing and testing solutions through experimentation. 8. Evaluating results to draw meaningful engineering conclusions.	8
	PO3	1. Understand customer and user needs while considering factors such as aesthetics. 2. Identify and manage cost drivers in engineering solutions. 3. Use creativity to develop innovative engineering solutions. 4. Ensure fitness for purpose across production, operation, maintenance, and disposal.	4
	PO4	1. Develop essential laboratory and workshop skills to carry out experimental investigations and gather reliable data.	6

		2. Address complex problems in various engineering contexts, including operations, management, and technology development. 3. Leverage technical literature and reliable information sources 4. Follow appropriate codes of practice and industry standards when analyzing and interpreting experimental data. 5. Ensure high-quality results by integrating various data sources and considering quality control during engineering investigations. 6. Draw valid conclusions by addressing technical uncertainties through sound reasoning and scientific principles.	
	PO5	1. Implement simulation tools in different engineering fields.	`1
	PSO1	1. Design of a circuit or system for a given specification	1
CO5	PO1	1. Integration of knowledge from various engineering disciplines.	1
	PO3	1. Investigate and define a problem while identifying constraints, including environmental, sustainability, health, and safety considerations. 2. Understand customer and user needs while considering factors such as aesthetics. 3. Identify and manage cost drivers in engineering solutions. 4. Use creativity to develop innovative engineering solutions. 5. Ensure fitness for purpose across production, operation, maintenance, and disposal. 6. Manage the design process and evaluate outcomes for safety and risk assessment.	6
	PO4	1. Gain a deep understanding of materials, equipment, processes, and products through research to address engineering problems effectively. 2. Develop essential laboratory and workshop skills to carry out experimental investigations and gather reliable data. 3. Address complex problems in various engineering contexts, including operations, management, and technology development.	6

		4. Leverage technical literature and reliable information sources 5. Follow appropriate codes of practice and industry standards when analyzing and interpreting experimental data. 6. Ensure high-quality results by integrating various data sources and considering quality control during engineering investigations.	
	PO5	1. Identify appropriate prediction and modelling tools for diverse engineering applications.	1
	PSO1	1. Analyze response of a circuit or system 2. Design of a circuit or system for a given specification 3. Understand and apply circuit or system specifications accurately. 4. Knowledge of analog and digital signal processing techniques.	4
	PSO2	1. Develop Operational block diagrams 2. Proficiency in the use of software tools for circuit design. 3. Hardware-software integration in communication systems 4. Understanding trade-offs in hardware and software design parameters.	4

<u>TOTAL COUNT OF KEY COMPETENCIES FOR CO – (PO, PSO) MAPPING:</u>

Course Outcomes	PROGRAM OUTCOMES												PSOs	
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2
	4	10	10	10	4	5	4	4	10	5	10	8	4	4
CO1	1	4	6	-	1	-	-	-	-	-	-	-	2	2
CO2	2	-	4	3	1	-	-	-	-	-	-	-	4	2
CO3	1	8	6	6	1	-	-	-	-	-	-	-	2	-
CO4	1	8	4	6	1	-	-	-	-	-	-	-	1	-

CO5	1	-	6	6	1	-	-	-	-	-	-	-	4	4

PERCENTAGE OF KEY COMPETENCIES FOR CO – (PO/ PSO):

Course Outcomes	PROGRAM OUTCOMES												PSOs	
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO 2
CO1	25	40	50	-	75	-	-	-	-	-	-	-	50	50
CO2	50	-	40	30	100	-	-	-	-	-	-	-	100	50
CO3	25	80	50	50	100	-	-	-	-	-	-	-	50	-
CO4	25	80	40	50	100	-	-	-	-	-	-	-	25	-
CO5	25	-	50	50	75	-	-	-	-	-	-	-	100	100

COURSE ARTICULATION MATRIX (PO – PSO MAPPING):

CO'S and PO'S, CO'S and PSO'S on the scale of 0 to 3, 0 being no correlation, 1 being the low correlation, 2 being medium correlation and 3 being high correlation.

0 - 0≤ C≤ 5% – No correlation,

1-5 <C≤ 40% – Low/ Slight

2 - 40 % <C< 60% –Moderate

3 - 60% ≤ C < 100% – Substantial /High

Course Outcomes	PROGRAM OUTCOMES												PSOs	
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO 1	PSO2
CO1	1	1	2	-	3	-	-	-	-	-	-	-	2	2
CO2	2	-	1	1	3	-	-	-	-	-	-	-	3	2
CO3	1	3	2	2	3	-	-	-	-	-	-	-	2	-
CO4	1	3	1	2	3	-	-	-	-	-	-	-	1	-
CO5	1	-	2	2	3	-	-	-	-	-	-	-	3	3
Total	6	7	8	7	15	-	-	-	-	-	-	-	11	7
Average	1.20	2.33	1.60	1.75	3	-	-	-	-	-	-	-	2.20	2.33

LAB TIME TABLE

ROOM NO: SR-110

NAME OF THE LAB: ICA LAB

A.Y: 2026-2027

BRANCH: ECE

W.E. F:

SEMESTER: V

<table>
<tr><th>PERIOD</th><th>1st</th><th>2nd</th><th>3rd</th><th rowspan="3">12:25 - 01:15</th><th>4th</th><th>5th</th><th>6th</th></tr>
<tr><td>TIME</td><td rowspan="2">09:40 - 10:35</td><td rowspan="2">10:35 - 11:30</td><td rowspan="2">11:30 - 12:25</td><td rowspan="2">01:15 - 02:10</td><td rowspan="2">02:10 - 03:05</td><td rowspan="2">03:05 - 04:00</td></tr>
<tr><td>DAY</td></tr>
<tr><td>MON</td><td colspan="3"></td><td rowspan="6">L
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H</td><td colspan="3"></td></tr>
<tr><td>TUE</td><td colspan="3"></td><td colspan="3"></td></tr>
<tr><td>WED</td><td colspan="3"></td><td colspan="3"></td></tr>
<tr><td>THU</td><td></td><td colspan="2"></td><td></td><td colspan="2"></td></tr>
<tr><td>FRI</td><td></td><td colspan="2"></td><td colspan="3"></td></tr>
<tr><td>SAT</td><td colspan="3"></td><td colspan="3"></td></tr>
</table>

Time Table I/C **Time Tables C/D** **HOD – ECE**

COURSE CONTENT

<table>
<tr><td colspan="9">INTEGRATED CIRCUITS APPLICATIONS LABORATORY</td></tr>
<tr><td colspan="9">V Semester: ECE</td></tr>
<tr><td rowspan="2">Course Code</td><td rowspan="2">Category</td><td colspan="3">Hours / Week</td><td>Credits</td><td colspan="3">Maximum Marks</td></tr>
<tr><td>L</td><td>T</td><td>P</td><td>C</td><td>CIA</td><td>SEE</td><td>Total</td></tr>
<tr><td>2450476</td><td>Core</td><td>0</td><td>0</td><td>2</td><td>1</td><td>40</td><td>60</td><td>100</td></tr>
<tr><td>Contact Classes: Nil</td><td>Tutorial Classes: Nil</td><td colspan="4">Practical Classes: 30</td><td colspan="3">Total Classes: 30</td></tr>
<tr><td colspan="9">Prerequisites: Basic concepts of linear and digital IC applications,</td></tr>
</table>

Couse Overview:

MATLAB plays a crucial role in Digital System Design Labs by providing essential tools and capabilities for simulation, algorithm development, testing, and education. Its versatility, ease of use, and integration with hardware platforms make it an indispensable tool for engineers and students alike in the field of digital system design. This Laboratory also serves as hardware implementation in various domains of digital system design, Signal and Image Processing, Data Visualization and Analysis, Control Systems Design, Machine Learning and Deep Learning, etc.

Course Objectives:

The students will try to learn

- The characteristics of op-amp
- Filter characteristics using IC741
- The operation of IC 555
- Designing of combinational circuits using ICs
- Implementation of the sequential circuits using ICs

Course Outcomes:

After successful completion of the course, students shall be able to

- Apply IC 741 and IC 555 in Practical Circuit Design
- Design and Implement Timer-Based Circuits Using IC 555
- Implement and Optimize IC 741 Filter Circuits for Signal Conditioning
- Analyze the Performance of Combinational Circuits
- Design sequential Circuits Using Digital ICs

List of Experiments:

1. Adder and Subtractor using Op Amp
2. Comparators using Op Amp.
3. Integrator and differentiator Circuits using IC 741.
4. Active Filter Applications –LPF, HPF (first order)
5. IC 741 Waveform Generators –Sine, Square wave and Triangular waves.
6. Mono-stable Multivibrator using IC 555
7. Three Terminal Voltage Regulators –7805, 7809, 7912
8. Design a 16-bit comparator using 4-bit Comparators.
9. Design a 450 KHz clock using NAND / NOR gates.
10. Design a 4-bit pseudo random sequence generator using 4 –bit ring counter.

11. Design a 16 x 1 multiplexer using 8 x 1 multiplexer.
12. Plot the transform Characteristics of 74H, LS, HS series IC's.
13. Design a 4 –bit Gray to Binary and Binary to Gray Converter
14. Design a Ring counter and Twisted ring counter using a 4-bit shift register
15. Design a 4-digit hex counter using synchronous one-digit hex counters

NOTE: Minimum of 12 experiments to be conducted

ELECTRONIC RESOURCES:

1. https://youtu.be/UznnkHMisIk
2. https://youtu.be/oRMfN0K9cWU
3. https://youtu.be/pgU-PZ8UZ3A
4. https://youtu.be/8YyYV8p1pE0
5. https://youtu.be/9b3xkFQpE5k
6. https://youtu.be/6Q9V4wZz9pQ
7. https://youtu.be/5qJm9Qk8n0U
8. https://youtu.be/4Yz2Z5QWn6A

MATERIALS ONLINE:

1. Lab Manual
2. Open-ended experiments

INTEGRATED CIRCUITS APPLICATIONS LABORATORY

LAB PLANNER

S.No	Experiment	CO	Virtual Lab Availability	Date planned	Date conducted
1	Adder and Subtractor using Op Amp	1	No		
2	Comparators using Op Amp.	1	No		
3	Integrator and differentiator Circuits using IC 741.	2	No		
4	Active Filter Applications –LPF, HPF (first order)	1	No		
5	IC 741 Waveform Generators –Sine, Square wave and Triangular waves.	1	No		
6	Mono-stable Multivibrator using IC 555	1	No		
	MID-I				
7	Design a 16-bit comparator using 4-bit Comparators.	5	No		
8	Design a 450 KHz clock using NAND / NOR gates.	5	No		
9	Design a 4-bit pseudo random sequence generator using 4 –bit ring counter.	4	No		
10	Design a 16 x 1 multiplexer using 8 x 1 multiplexer.	4	No		
11	Plot the transform Characteristics of 74H, LS, HS series IC’s.	4	No		
12	Design a 4 –bit Gray to Binary and Binary to Gray Converter	4	No		
13	Design a Ring counter and Twisted ring counter using a 4-bit shift register	4	No		
	MID-II				

INTEGRATED CIRCUITS APPLICATIONS LABORATORY

LAB PLANNER

Date planed																			
Date conducted																			
Roll Number	**Exp No**	**CO**	**VL**	**Exp No**	**CO**	**VL**	**Exp No**	**CO**	**VL**	**Exp No**	**CO**	**VL**	**Exp No**	**CO**	**VL**	**Exp No**	**CO**	**VL**	
	1	1	N	2	1	N	3	2	N	4	1	N	5	1	N	6	1	N	
	1	1	N	2	1	N	3	2	N	4	1	N	5	1	N	6	1	N	**M**
	1	1	N	2	1	N	3	2	N	4	1	N	5	1	N	6	1	N	**I**
	1	1	N	2	1	N	3	2	N	4	1	N	5	1	N	6	1	N	**D**
	1	1	N	2	1	N	3	2	N	4	1	N	5	1	N	6	1	N	**-**
	1	1	N	2	1	N	3	2	N	4	1	N	5	1	N	6	1	N	**I**

Note: VL*-Virtual Lab Availability

Date planed																			
Date conducted																			
Roll Number	**Exp No**	**CO**	**VL**	**Exp No**	**CO**	**VL**	**Exp No**	**CO**	**VL**	**Exp No**	**CO**	**VL**	**Exp No**	**CO**	**VL**	**Exp No**	**CO**	**VL**	
	7	4	Y	8	4	Y	9	4	Y	10	4	Y	11	4	Y	12	5	Y	
	7	4	Y	8	4	Y	9	4	Y	10	4	Y	11	4	Y	12	5	Y	**M**
	7	4	Y	8	4	Y	9	4	Y	10	4	Y	11	4	Y	12	5	Y	**I**
	7	4	Y	8	4	Y	9	4	Y	10	4	Y	11	4	Y	12	5	Y	**D**
	7	4	Y	8	4	Y	9	4	Y	10	4	Y	11	4	Y	12	5	Y	**-**
	7	4	Y	8	4	Y	9	4	Y	10	4	Y	11	4	Y	12	5	Y	**II**

Note: VL*-Virtual Lab Availability

INTEGRATED CIRCUITS APPLICATIONS LABORATORY

RUBRICS USED TO ASSESS LEARNINGS IN LABORATORIES

1. RUBRICS FOR DAY TO DAY EVALUATION

Parameter	Max Marks	Level-1 (Very Poor)	Level-2 (Poor)	Level-3 (Average)	Level-4 (Good)	Level-5 (Excellent)
Observation Book	05	No observations or irrelevant data. (0–1)	Incomplete or incorrect data. (2)	Basic values with some errors. (3)	Mostly correct with good format. (4)	Fully correct, clear, and well-formatted. (5)
Record Writing	05	Not submitted. (0-1)	Submitted but mostly incomplete. (2)	Submitted with some missing/wrong parts. (3)	Submitted with minor issues. (4)	Fully complete, correct algorithm & flowchart. (5)
Result	05	No result or major errors. (0–1)	Result partially obtained. (2)	Acceptable result with limited error. (3)	Near-correct result and reasonable error. (4)	Accurate result. (5)
Viva-Voce	05	Did not answer any questions. (1)	Answered very few questions. (2)	Answered some questions with help. (3)	Answered most questions correctly. (4)	Answered all questions accurately. (5)

INTEGRATED CIRCUITS APPLICATIONS LABORATORY

2. RUBRICS FOR INTERNAL EVALUATION

Criterion	Max Marks	Level-1 *(Very Poor)*	Level-2 *(Poor)*	Level-3 *(Average)*	Level-4 *(Good)*	Level-5 *(Excellent)*
Design/Tool/Apparatus Selection	2 Marks	Incorrect tool/design and no reasoning. **(0)**	Tool/design selection attempted with unclear logic. **(0.5)**	Satisfactory selection with partial justification. **(1)**	Correct selection and proper analysis with few errors. **(1.5)**	Smart selection with accurate, relevant analysis. **(2)**
Execution (Code/Debug/Run) /Analysis/Method Used	4 Marks	Did not attempt or completely failed to execute. **(0)**	Attempted but unable to proceed or with major errors. **(1)**	Partial execution with some logic/syntax errors. **(2)**	Mostly correct execution with minimal help. **(3)**	Fully correct and independently executed program. **(4)**
Results& Documentation	2 Marks	Incomplete or poorly presented. **(0)**	Basic structure but lacks clarity or formatting. **(0.5)**	Complete but generic or with formatting issues. **(1)**	Well-structured and mostly clear. **(1.5)**	Well-organized, professional, and engaging documentation. **(2)**
Viva-Voce (Understanding of Concepts)	2 Marks	No understanding; could not answer questions. **(0)**	Answered a few with difficulty. **(0.5)**	Answered half the questions with basic clarity. **(1)**	Good understanding with confident answers. **(1.5)**	Answered all questions with clarity and depth. **(2)**

INTEGRATED CIRCUITS APPLICATIONS LABORATORY

3.RUBRICS FOR SEMESTER END EXAMINATIONS

Criterion	Max Marks	Level-1 (Very Poor *(0–2 marks)*	Level-2 (Poor)*(3–4 marks)*	Level-3 (Average)*(5–6 marks)*	Level-4 (Good)*(7–9 marks)*	Level-5 (Excellent)*(10–12 marks)*
Preparedness for the Experiment	12 marks	No clarity on objective or procedure. Unable to explain basics.	Limited idea of the objective/procedure. Needed prompting.	Has basic understanding; minor gaps in concept or preparation.	Well-prepared, with clear understanding of steps and background.	Fully prepared with strong conceptual clarity and confident explanation.
Performance in the Laboratory	12 marks	Unable to perform experiment. Relied entirely on examiner's help.	Performed with multiple errors and constant support.	Performed with some errors; required occasional help.	Performed mostly independently with minimal support.	Performed independently, efficiently, and with precision.
Calculations & Graphs	12 marks	No or incorrect calculations. Graphs missing or irrelevant.	Multiple calculation errors. Graphs/ plots inaccurate or poorly labelled.	Calculations partially correct. Graphs present but with some flaws.	Correct calculations and graphs with minor errors.	Accurate calculations and well-labelled graphs with proper interpretation.
Results & Error Analysis	12 marks	No result or invalid result. No error analysis attempted.	Incorrect result with vague or no error discussion.	Acceptable result. Error analysis attempted but limited.	Correct result with sound error discussion.	Accurate result with detailed and relevant error analysis.

Viva-Voce (Subject Knowledge)	12 marks	Unable to answer any questions. No conceptual understanding.	Answered few questions with poor logic.	Answered half of the questions with average understanding.	Answered most questions with clarity and confidence.	Answered all questions with depth, clarity, and reasoning.

INDEX

Department of Electronics & Communication Engineering

B.Tech. ECE-III -I Sem

ICA LAB

Note:Minimumof12experiments

Verify the functionality of the IC in the application

ICA LAB: Experiments

1. Adder and Subtractor using Op Amp
2. Comparators using Op Amp.
3. Integrator and differentiator Circuits using IC741.
4. Active Filter Applications –LPF, HPF (first order)
5. IC 741 Waveform Generators –Sine, Square wave and Triangular waves.
6. Mono-stable Multivibrator using IC555
7. Three Terminal Voltage Regulators –7805, 7809,7912
8. Design a 16-bit comparator using 4-bit Comparators.
9. Design a 450 KHz clock using NAND / NOR gates.
10. Design a 4-bit pseudo random sequence generator using 4 –bit ring counter.
11. Design a 16 x 1 multiplexer using 8 x 1multiplexer.
12. Plot the transform Characteristics of 74H, LS, HS series IC's.
13. Design a 4 –bit Gray to Binary and Binary to Gray Converter
14. Design a Ring counter and Twisted ring counter using a 4-bit shift register
15. Design a 4-digit hex counter using synchronous one-digit hex counters.

EQUIPMENTREQUIRED:

1. 20MHz/40MHz/60MHzOscilloscopes.
2. 1MHzFunctionGenerator(Sine, Square, Triangular and TTL).
3. Regulated Power Supply.
4. Multimeter/Volt-Meter.

EXPERIMENTNO:1

ADDER AND SUBTRACTOR USING OP AMP.

AIM: To study Adder & Subtractor circuits using OP-AMPIC741and verify their theoretical and practical output.

PRELAB:

1. Study the purpose of using Operational amplifiers.
2. Learn the different Configuration of Operational amplifiers.
3. Identify all the formulae you will need in this Lab.

OBJECTIVE:

After completion of this experiment student will be able to

- To Design and setup a Summing amplifier using op-amp
- To Ddetermine the output voltages by providing different dc input voltages

APPARATUS: Breadboard
IC741,Resistors
DC Supply
Function Generator
Multimeter
CRO
Probes, Connecting Wires

THEORY:

Adder: Op-amp can be used to design a circuit whose output is the sum of several input signals. Such a circuit is called a summing amplifier or an adder. Summing amplifier can be classified as inverting & non-inverting summer depending on the input applied to inverting & non-inverting terminals respectively .Here the output will be the linear summation of input voltages.

The circuit can be used either as summing amplifier, scaling amplifier, Or as averaging amplifier.

$$V_0=V_1+V_2+V_3+\ldots+V_n$$

This means that the output voltage is equal to the sum of all the input voltages.

Subtractor: A Subtractor is a circuit that gives the difference of the two inputs, $V_O = V_2 - V_1$, Where V_1 and V_2 are the inputs. By connecting one input voltage V_1 to inverting terminal and Another input voltage V_2 to the non–inverting terminal, we get the resulting circuit as the Subtractor. This is also called as differential or difference amplifier using op-amps.
Output of a differential amplifier (subtractor) is given as

$$V_o = \left[\frac{-R_f}{R_1}\right](V_1 - V_2) \quad \text{(1)}$$

If all external resistors are equal in value, then the gain of the amplifier is equal to -1. The output voltage ofthedifferentialamplifierwithagainof-1is

$$V_o = (V_2 - V_1) \quad \text{(2)}$$

Thus, the output voltage V_O is equal to the voltage V_2 applied to the non–inverting terminal minus the voltage V_1 appliedtotheinvertingterminal.HencethecircuitiscalledaSubtractor.

CIRCUITDIAGRAM:

Adder:

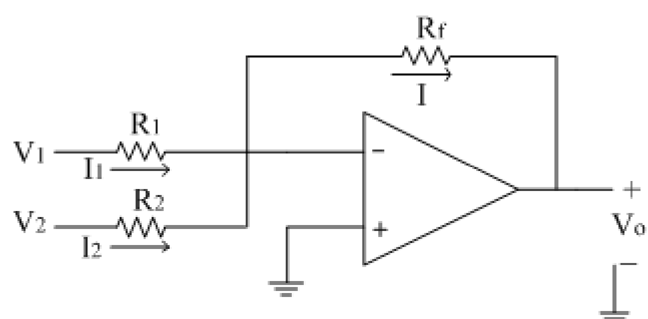


Fig :2.1 circuit diagram of adder

Subtractor

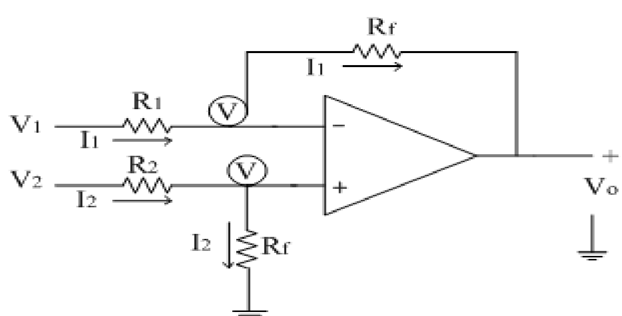


Fig :2.2 circuit diagram of subtractor

PROCEDURE:

Adder:

1. Connect the components/equipment as shown in the circuit diagram.
2. Switch ON the power supply.
3. Apply dc voltages at each input terminal for V_1 and V_2 from the dc supply and check the output voltage V_o at the output terminal.
4. Tabulate 3 different sets of readings by repeating the above step.
5. Compare practical V_o with the theoretical output voltage $V_o=V_1+V_2$.

Subtractor:

1. Connect the components / equipment as shown in the circuit diagram.
2. Switch ON the power supply.
3. Apply dc voltages at each input terminal for V_1 and V_2 from the dc supply and check the output voltage V_o at the output terminal.
4. Tabulate 3 different sets of readings by repeating the above step.
5. Compare practical V_o with the theoretical output voltage $V_o=V_2-V_1$.

Tabular Column:

Adder:

S.No.	**V1 Volts**	**V2 Volts**	**Theoretical $V_o=V_1+V_2$**	**Practical VoVolts**

Subtractor:

S.No.	**V1 Volts**	**V2 Volts**	**Theoretical $V_o=V_2-V_1$**	**Practical VoVolts**

RESULT: Adder & Subtractor circuits using OpAMP IC741andverify their theoretical and practical output.

Viva Question’s:

1. Draw the circuit diagram of 3 input adder.
2. What is the other name for adder?
3. Draw the circuit diagram of a Subtractor.
4. Which amplifier acts as a Subtractor?
5. Draw an op-amp circuit whose output V_O is $V_1+V_2-V_3-V_4$.
6. What is operational amplifier?
7. Define Adder?
8. Define Subtractor?
9. What is the output of subtractor ?
10. What are the applications of op-amp?
11. What is the input impedance of ideal op-amp?
12. What is the output impedance of ideal op-amp?
13. What is the slew rate of ideal op-amp?
14. What is the bandwidth of idea lop-amp?
15. Op-amp was introduced in which year?
16. By using what the OP-amp was designed?
17. Why it is called as op-amp?
18. Who was invented IC741op-amp?
19. Advantages of op-amp?
20. Dis-advantages of op-amp?
21. Op-amp is also called as?
22. What is the gain of inverting op-amp if Rf=10k&R1=1k?
23. What is the gain of non-inverting op-amp if Rf=10k&R2=1k?
24. What is the output of subtractor if V1=1v & V2=3v?
25. What is negative feedback in op-amp?
26. What is positive feedback in op-amp?
27. What is open loop configuration of op-amp?
28. What is closed loop configuration of op-amp?
29. What are the DC characteristics of op-amp?
30. What are the liner applications of op-amp?
31. What are the non-linear applications of op-amp?
32. What is the non-inverting op-amp?
33. What is inverting op-amp?
34. What is frequency response?
35. Why we cannot fabricate inductors on IC?
36. What is the range of capacitors, we cannot fabricate on IC?
37. Can we replace new components on IC?
38. Which material is used to fabricate IC?
39. Formula to calculate voltage across capacitor?
40. Difference between non-inverting & inverting op-amp?
41. What is formula to calculate voltage across resistor?
42. What is formula to calculate voltage across the capacitor?
43. Classifications of IC's?

44. Based on level of integration IC is classified as?
45. Based on mode of operation IC is classified as?
46. Based on fabrication IC is classified as?
47. Range of components fabricated on large Scale IC?
48. Range of components fabricated on very large-scale IC?
49. Range of components fabricated on ultra-large-scale IC?
50. What is the output of inverting adder if Theis are V1, V2, V3

REAL TIME APPLICATIONS:

1. Op-Amp Adder-mix bus summing amplifier as used in audio mixing consoles.
2. Op-Amp Subtractor-Differential amplifier: remove common-mode signal from a differential signal source.
3. Voltage Adder (Summing Amplifier): For Noise Cancellation, Audio Mixer, Digital to Analog Converter (DAC) Level Shifter.

EXPERIMENTNO:2

DATE:COMPARATORSUSINGOPAMP.

AIM: To study comparators using OP-AMP IC741 and verify their theoretical and practical output.

PRELAB:

1. Study the purpose of using Operational amplifiers.
2. Learn about Differential Operational amplifiers
3. Identify all the formulae you will need in this Lab.

OBJECTIVE:

After completion of this experiment student will be able to

- To Design and setup a Comparator using op-amp
- To Determine the output voltages by providing different reference voltages and input voltages

APPARATUS: Bread Board
IC741,Resistors
DC Supply
Function Generator
Multimeter
CRO
Probes, Connecting Wires

THEORY:

A Comparator is a non-linear signal processor. It is an open loop mode application of Op-amp operated in saturation mode. Comparator compares a signal voltage at one input with a reference voltage at the other input. Here the Op-amp is operated in open loop mode and hence the output is $\pm V_{sat}$. It is basically classified as inverting and non-inverting comparator. In a non-inverting comparator V_{in} is given to +ve terminal and V_{ref} to –ve terminal. When $V_{in}<V_{ref}$, the output is $-V_{sat}$ and when $V_{in} > V_{ref}$, the output is $+V_{sat}$ (see expected waveforms). In an inverting comparator input is given to the inverting terminal and reference voltage is given to the non-inverting terminal. The output of the inverting comparator is the inverse of the output of non-inverting comparator. The comparator can be used as a zero-crossing detector, window detector, time marker generator and phasemeter.

CIRCUITDIAGRAM:

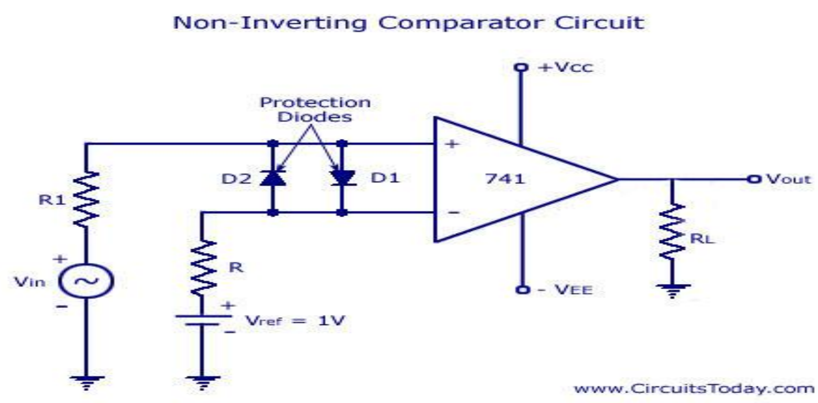


Fig: Circuit diagram of comparator

PROCEDURE:

1. Connect the components / equipment as shown in the circuit diagram.
2. Switch ON the power supply.
3. Apply 1KHz sinewave with $5V_{pp}$ at the non-inverting input terminal of IC741 using a function generator.
4. Apply 1Vdc voltage as reference voltage at the inverting terminalofIC741.
5. Connect the channel-1 of CRO at the input terminals and channel-2 of CRO at the output terminals.
6. Observe the input sinusoidal signal at channel-1 and the corresponding output square wave at channel-2 of CRO. Note down their amplitude and time period.
7. Overlap both the input and output waves and note down voltages at positions on sinewave where the output changes its state. These voltages denote the Reference voltage.
8. Plot the output square wave corresponding to the sine input with V_{ref}=1V.

Comparator Observation Table:

Theoretical Reference voltage (from circuit)	
Practical Reference voltage (from output waveforms)	

EXPECTEDWAVEFORMS:

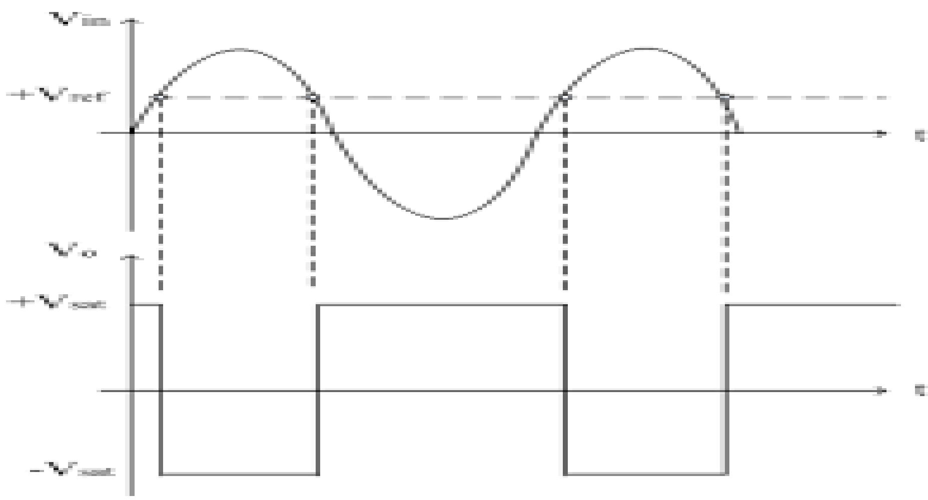


Fig : Input and output waveforms of inverting comparator

RESULT: comparators using OP-AMP IC741andverifytheirtheoreticalandpracticaloutput

Viva Question's:

1. How many basic input parameters are required for comparator?
2. Draw the circuit diagram of a non-inverting comparator and inverting comparator.
3. What is the output of a non-inverting comparator and inverting comparator if the input is sinusoidal?
4. What are the differences between the Inverting and Non–Inverting comparator?
5. What is the name of the comparator if the reference voltage is 0V?
6. Draw the circuit diagram and the output waveform of a Zero Crossing Detector if the input is sinusoidal?
7. What is the name of a regenerative comparator?
8. Draw an op-amp circuit whose output V_o is $V_1+V_2-V_3-V_4$.
9. Define comparator?
10. What are the types of comparators?
11. In which configuration of op-amp does a comparator works?
12. Define an operational amplifier?
13. Define integrated circuit?
14. What are applications of comparator?
15. What is another name of comparator?
16. What operational does a comparator perform?
17. What are the differences between open loop & closed loop Configuration?
18. What are applications of IC's?
19. What are applications of operational Amplifier?
20. What does comparator generate when Vin<V>ref?
21. What output does comparator generates when Vin>Vref?
22. What are the real-time applications of comparator?
23. How many input parameters are required for comparator?
24. Draw the circuit of inverting &non-inverting comparator?
25. What are the differences between inverting & non-inverting Comparator?
26. What is the gain of non-inverting op-amp?
27. What is the gain of inverting op-amp?
28. What are linear applications of op-amp?
29. What are non-linear applications of op-amp?
30. What are applications of open loop configuration?
31. Define feedback?
32. Define positive feedback?
33. Define Negative feedback?
34. What are the differences between positive & negative feedback?
35. Who invented IC741?
36. Why it is named as op-amp?
37. Why it is named as comparator?
38. What are advantages of op-amp?
39. What are advantages of IC's?

40. Define amplifier?
41. Define differential amplifier?
42. Define CMRR?
43. Define slew rate?
44. Define thermal drift?
45. Define bandwidth?
46. What are the characteristics of differential amplifier?
47. Why comparator is called voltage level detector?
48. What is the name of comparator if reference voltage is 0V?

REAL TIME APPLICATIONS

A comparator consists of a specialized high-gain differential amplifier. They are commonly used in devices that measure and digitize analog signals, such as analog-to-digital converters (ADCs) and relaxation oscillators.

Comparator circuits are used in designing electrical and electronics projects (like Temperature Humidity Monitoring System, Smoke Alarm Circuit).

EXPERIMENT NO:3 DATE:

INTEGRATOR AND DIFFERENITATOR CIRCUIT USING IC741 OP-AMP

EXPERIMENT:3A

INTEGRATOR CIRCUIT USING IC741 OP-AMP

AIM: To study the operation of the Integrator circuit using op-amp and trace the output waveforms for sine and square wave inputs.

PRELAB:

1. Study the purpose of using Operational amplifiers
2. Learn the different types of Op-amp Configuration methods.
3. Identify all the formulae you will need in this Lab.

OBJECTIVES:

After completion of this experiment student will be able to
To design and setup an Integrator using op-amp
To determine the output voltages by providing different R and C values
To plot the frequency response of an integrator circuit

APPARATUS: Breadboard
IC741, Resistors, Capacitors
Function Generator
CRO
Probes
Connecting wires

THEORY:

Integrator:

A circuit in which the output voltage is the integration of the input voltage is called an integrator.

$$V_o = -\frac{1}{R_1C_1}\int V_{in}\,dt \quad \rightarrow (1)$$

In the practical integrator to reduce the error voltage at the output, a resistor R_f is connected across the feedback capacitor C_F. Thus, R_F limits the low-frequency gain and hence minimizes the variations in the output voltage.

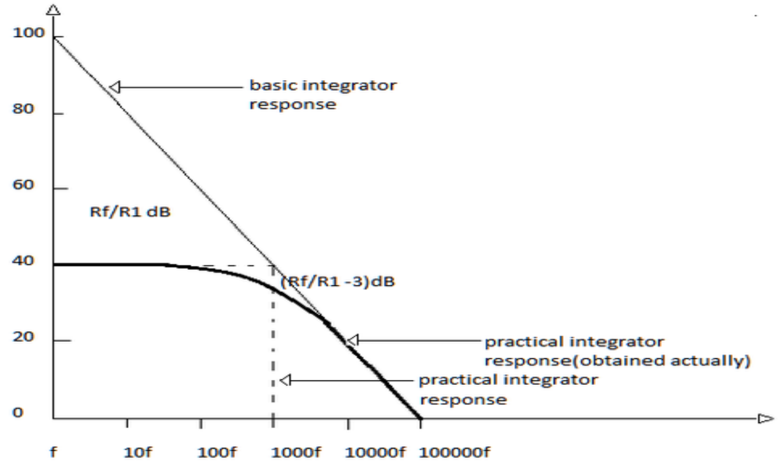


Fig 4.1 Frequency response of Integrator

The frequency response of the integrator is shown in the fig. 2.1. f_b is the frequency at which the gain is 0dB and is given by

$$f_b = \frac{1}{2\pi R_1 C_1} \quad (2)$$

In this fig. there is some relative operating frequency, and for frequencies from f to f_a the gain R_F/R_1 is constant. However, after f_a the gain decreases at a rate of 20 dB/decade. In other words, between f_a and f_b the circuit of fig. 2.1 acts as an integrator. The gain-limiting frequency f_a is given by

$$f_a=1/2\square R_fC_f. \quad (3)$$

Normally $f_a<f_b$. From the above equation, we can calculate R_f by assuming f_a & C_f. This is very important frequency. It tells us where the useful integration range starts.

If $f_{in}<f_a$ -circuit acts like a simple inverting amplifier and no integration results,
If $f_{in}=f_a$ -integration takes place with only 50% accuracy results,
If $f_{in}=10f_a$ -integration takes place with 99% accuracy results.

In the circuit diagram of Integrator, the values are calculated by assuming f_a as50Hz. Hence the input frequency is to be taken as 500Hz to get 99% accuracy results.

CIRCUIT DIAGRAM:

Integrator:

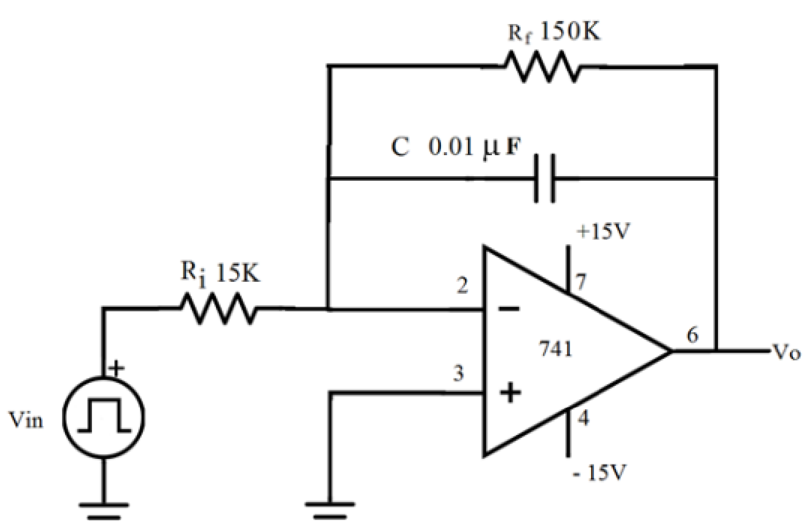


Fig : Circuit diagram of Integrator

PROCEDURE:

Integrator:

1. Connect the components/equipment as shown in the circuit diagram.
2. Switch ON the power supply.
3. Apply sine wave at the input terminals of the circuit using function Generator.
4. Connect channel-1of CRO at the input terminals and channel-2 at the output terminals.
5. Observe the output of the circuit on the CRO which is a cosine wave(90^o phase shifted from the sine wave input)and note down the position, the amplitude and the time period of V_{in}&V_O.
6. Now apply the square wave as input signal.
7. Observe the output of the circuit on the CRO which is a triangular wave and note down the position, the amplitude and the time period of V_{in}&V_O.
8. Plot the output voltages corresponding to sine and square wave inputs.

EXPECTED WAVEFORMS:

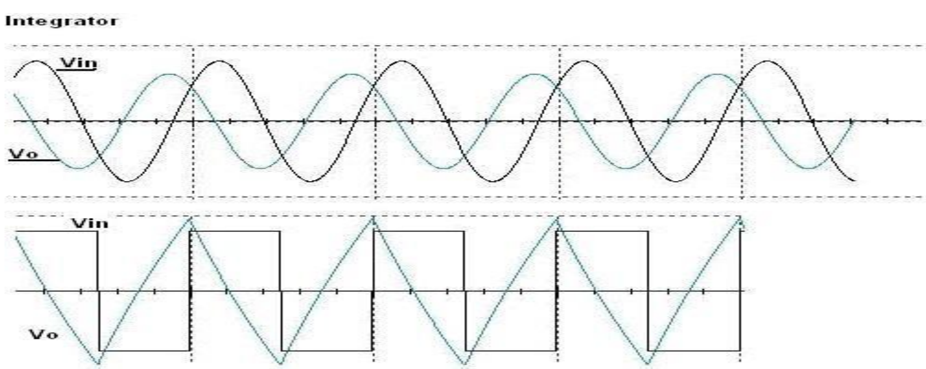


Fig 4.3 Output waveforms of Integrator

RESULT: Verify the operation of the Integrator circuit using op-amp and trace the output waveforms for sine and square wave inputs

QUESTIONS:

1. What is an Integrator?
2. Draw the circuit of the Integrator usingop-ampIC741.
3. Write down the expression for V_O of an Integrator.
4. Draw the frequency response of the Integrator and explain.
5. Draw the output waveform of the Integrator when the input is a square wave.
6. What is the purpose behind the connection of Rf in the feedback path of Integrator?
7. What are the applications of Integrator?
8. How does integrator acts?
9. Integrator converts square wave to wave? Bandwidth formula ?
10. At which frequency gain of integrator is constant?
11. Which feedback is used in integrator?
12. Applications of integrator?
13. Which ic is used in integrator circuit?
14. If frequency is integrator circuit?
15. If frequency is increased than the gain of integrator is increased(or) decreased?
16. What is formulas for FH?
17. What is the application of closed loop feedback?
18. What are advantages closed loop feedback?
19. Define bandwidth?
20. Define frequency response?
21. At which pin we are taking output?
22. At which pin we are giving input to the integrator?
23. Formula for the gain?
24. Define ic?
25. Advantage of IC’s?
26. Disadvantage of ICs?
27. Integrator is amplifier?
28. Formula for the gain of inverting amplifier?
29. Formula for the gain of non-inverting amplifier?
30. Define op-amp?
31. Difference between closed loop and open loop feedback?
32. Difference between inverting amplifier op-amp and non-op-amp
33. Draw the circuit of the integrator using op-amp?
34. Draw the frequency response of the integrator?
35. Define slew rate?
36. Define CMRR?
37. Define low pass filter?
38. Define high pass filter?
39. Define filter?
40. Draw the output wave form for integrator?
41. What is passive filter?
42. What is active filter?
43. Application of the filter
44. Define the feedback
45. Define the roll off
46. What is the range for semi log graph?
47. Define the frequency response plot
48. At low frequency the output of integrator?
49. At high frequency the output of integrator

50. Define frequency?

EXPERIMENTNO:3B

DIFFERENTIATORCIRCUITUSINGIC741OP-AMP

AIM: To study the operation of the differentiator circuit using op-amp and trace the output waveforms for sine and square wave inputs.

PRELAB:

1. Study the purpose of Differentiator using Operational amplifiers
2. Learn about inverting and Non inverting Configurations.
3. Identify all the formulae you will need in this Lab.

OBJECTIVES:

After completion of this experiment student will be able to
To design and setup a Differentiator using op-amp
To determine the output voltages by providing different R and C values
To plot the frequency response of an integrator circuit

APPARATUS:
Breadboard
IC741, Resistors, Capacitors
Function Generator
CRO
Probes
Connecting wires

THEORY:

Differentiator:

As the name suggests, the circuit performs the mathematical operation of differentiation, i.e. the output voltage is the derivative of the input voltage.

$V_o = -R_f C_1 dV_{in}/dt$ → (1)

Both the stability and the high-frequency noise problems can be corrected by the addition Of two components: R_1 and C_f, as shown in the circuit diagram.
This circuit is a practical differentiator.
The input signal will be differentiated properly if the time period T of the input signal is larger than or equal to $R_f C_1$.That is, $T >= R_f C_1$
Differentiator can be designed by implementing the following steps.
Select f_a equal to the highest frequency of the input signal to be differentiated. Then, assuming a value of $C_1 < 1$ □F, calculate the value of R_f

1. Calculate the values of R_1 and C_f so that $R_1C_1=R_fC_f$.

CIRCUITDIAGRAM:

Differentiator:

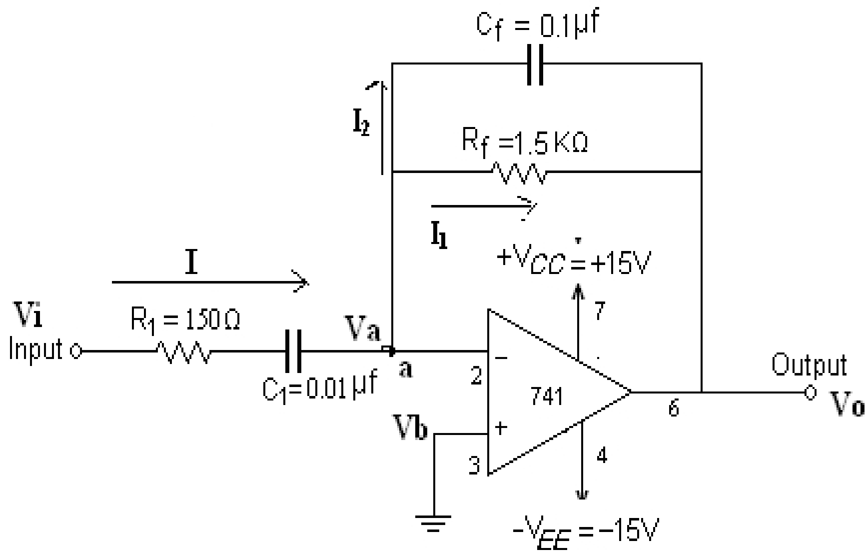


Fig 5.1 Circuit diagram of Differentiator

PROCEDURE:

Differentiator:

- Connect the components/equipment as shown in the circuit diagram.
- Switch ON the power supply.
- Apply sine wave at the input terminals of the circuit using function Generator.
- Connect channel-1of CRO at the input terminals and channel-2 at the output terminals.
- Observe the output of the circuit on the CRO which is a cosine wave (90^{o} phase shifted from the sine wave input) and noted own the position, the amplitude and the time period Of V_{in}&V_o.
- Now apply the square wave as input signal.
- Observe the output of the circuit on the CRO which is a spike wave and note down the position, the amplitude and the time period of V_{in}&V_o.
- Plot the output voltages corresponding to sine and square wave inputs.

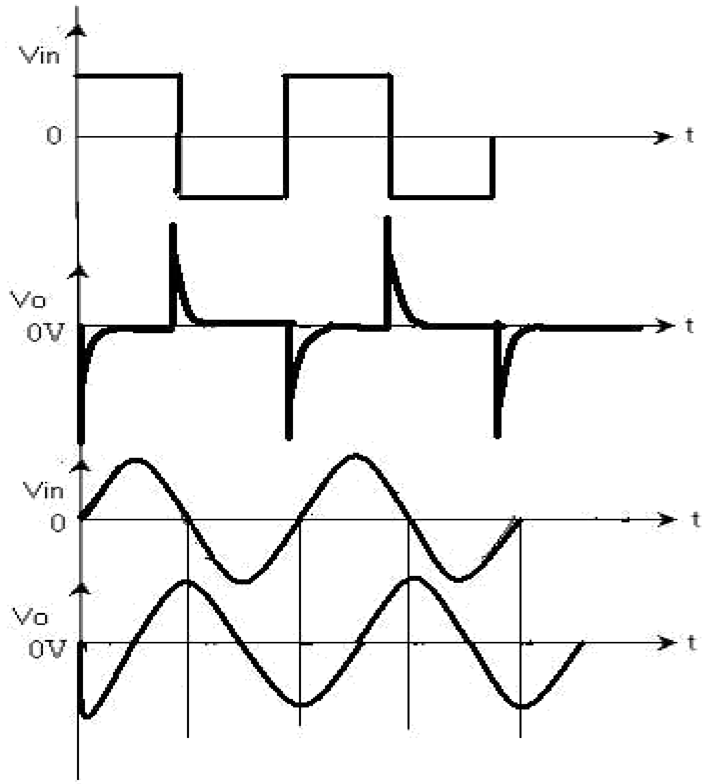


Fig 5.2Output waveform of Differentiator

RESULT: Verify the operation of the Differentiator circuit using op-amp and trace the output waveforms for sine and square wave inputs

Viva Question's:

1. Why R comp is used in both Integrator and Differentiator circuits?
2. What is a Differentiator?
3. Draw the circuit of the Differentiator using op-amp IC741.
4. Write down the expression for Vo of a Differentiator.
5. Draw the output waveform of the Differentiator when the input is a Sinewave.
6. Why R1 and Cf are connected in the circuit of the Differentiator?
7. What are the applications of Differentiator?
8. Formula for the gain of inverting amplifier?
9. Formula for the gain of non-inverting amplifier?
10. Define op-amp?
11. Difference between closed loop and open loop feedback?
12. Difference between inverting amplifier op-amp and non-op-amp
13. Draw the circuit of the integrator using op-amp?
14. Draw the frequency response of the integrator?
15. Define slew rate?
16. Define CMRR?
17. Define lowpass filter?
18. Define high pass filter?

19. How does integrator acts?

20. Integrator converts square wave to wave?
21. Bandwidth formula ?
22. At which frequency gain of integrator is constant?
23. Which feedback is used in integrator?
24. Define amplifier?
25. Define differential amplifier?
26. Define CMRR?
27. Define slew rate?
28. Define thermal drift?
29. Define band width?
30. What are the characteristics of differential amplifier?
31. Why comparator is called voltage level detector?
32. What is the name of comparator if reference voltage is 0V?
    a. What are formulae for gain of amplifier
    b. Why R1 and C fa reconnected in the circuit of the Differentiator?
33. What are the applications of Differentiator?
34. Formula for the gain of inverting amplifier?
35. What is the gain of inverting op-amp if Rf=10k&R1=1k?
    a. What is the gain of non-inverting op-amp if Rf=10k&R2=1k?
36. What is the output of subtractorifV1=1v&V2=3v?
37. What is negative feedback in op-amp?
38. What is positive feedback in op-amp?
39. What is open loop configuration of op-amp?
40. What is closed loop configuration of op-amp?
41. What are the DC characteristics of op-amp?
42. DrawthecircuitoftheDifferentiatorusingop-ampIC741.
43. Write down the expression for Vo of a Differentiator.
44. Draw the output wave for m of the Differentiator when the input is a Sine wave.
45. Why R1 and C fa reconnected in the circuit of the Differentiator?
46. What are the applications of Differentiator?
47. What is the output of subtractor if V1=1v&V2=3v?
48. What is formulae for gain of amplifier?
49. What are formulae for output voltage of differential amplifier?
50. Define low pass filter?

REAL TIME APPLICATIONS

The op-amp integrator has many applications and uses the most common of which is in calculus operations in analog computers, ramp generators, wave shaping circuits, and A/D converters.

Differentiating amplifiers are most commonly designed to operate on triangular and rectangular signals.

Differentiators also find application as wave shaping circuits, to detect high frequency components in the input signal.

EXPERIMENTNO: 4

ACTIVE FILTER APPLICATIONS-LPF&HPF(1STORDER)

EXPERIMENTNO:4A
a) 1st Order LOW PASS FILTER:

AIM: To plot the frequency response of Butter worth LPF(First order)and find the high cut-off exp? frequency.

PRELAB:

1. Study the purpose of using Operational amplifiers
2. Learn about Active Low Pass Filters
3. Identify all the formulae you will need in this Lab.

OBJECTIVES:

After completion of this experiment student will be able to
To Design and setup a Differentiator using op-amp
To Ddetermine the output voltages by providing different R and C values
To plot the frequency response of an integrator circuit

APPARATUS: Bread Board
Function Generator
CRO Probes
Connecting Wires
741Op-amp, Resistors, Capacitors

THEORY:

Filters are classified as follows:
Based on components used in the circuit

- Active filters–Use active elements like transistor or op-amp(provides gain) in addition to passive elements
- Passive filters–Use only passive elements like resistors, capacitors and inductors.

Based on frequency range

- Low pass filter (LPF) –Allows low frequencies
- High pass filter (HPF)–Allows high frequencies
- Bandpass filter (BPF)–Allows band of frequencies
- Band reject filter (BRF)–Rejects band of frequencies All pass filter – Allows all frequencies but with a phase shift

Active Filter is often a frequency – selective circuit that passes a specified band of frequencies and blocks or attenuates signals of frequencies outside this band.

These Active Filters are most extensively used in the field of communications and signal processing. They are employed in one form or another in almost all sophisticated electronic systems such as Radio, Television, Telephone, Radar, Space Satellites, and Bio-Medical Equipment.

Active Filters employ transistors or Op– Amps in addition to that of resistors and capacitors. Active filters have the following advantages over passive filters. (1) Flexible gain and frequency adjustment. (2) No loading problem (because of high input impedance and low output impedance) and Active filters are more economical than passive filters.
A first – Order Low – Pass Butterworth filter uses RC network for filtering. Note that the op-amp is used in the non – inverting configuration; hence it does not load down the RC network

Resistors R_1 and R_F determine the gain of the filter.

The gain magnitude equation of the Low–Pass filter can be obtained by converting equation into its equivalent polar form, as follows.

$$|V_o/V_{in}| = A_F/\sqrt{1+(f/f_H)^2}$$

Where 1

f_H= = high cut – off frequency of the filter.
2 ∏RC

The operation of the low– pass filter can be verified from the gain magnitude equation.

1. At very low frequencies, that is $f<f_H$

$$|V_o/V_{in}| = A_F$$

2.At $f=f_H$, $|V_o/V_{in}| = A_F/\sqrt{2}=0.707A_F$

3.At $f>f_H$ $|V_o/V_{in}| < A_F$

Thus, the Low – Pass filter has a constant gain A_F from 0 Hz to the almost high cut-off frequency, f_H, it has the gain $0.707A_F$ at exactly f_H, and after f_H it decreases at a constant rate withanincreaseinfrequency.Thegaindecreases20 dB(=20 log 10)each time the frequency is increased by10.Hencetherateat which the gain rolls off after f_H is20dB/decade. The frequency $f=f_H$ is called the cut-off frequency because the gain of the filter at this frequency is down by 3dB(=20log0.707) from 0Hz. Other equivalent terms for cut-off frequency are-3dB frequency, break frequency ,or corner frequency.

DESIGN:

1. Choose a value for high cut-off frequency, f_H (1 K Hz)and a value for gain, A_F (2)
2. Assume a value of C 1µF(0.1µF)
3. Calculate the value of R using the equation
4. Finally, select values of R_1 and R_F dependent on the desired pass band gain $A_F$using

   1
5. Assume a value for R_1(10KΩ) and calculate R_F.

CIRCUITDIAGRAM:

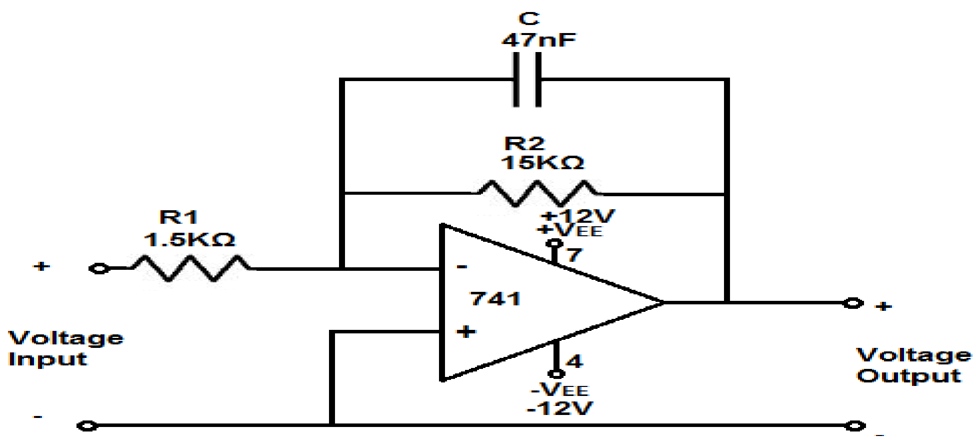


Fig: Active LowPass Filter

PROCEDURE:

1. Connect the components/equipment as shown in the circuit diagram.
2. Switch ON the power supply.
3. Connect channel -1 of CRO to input terminals (V_{in}) and channel -2 to output terminals(V_o).
4. Set V_{in}=1V&f_{in}=10Hz using function generator.
5. By varying the input frequency in regular intervals, noted down the output voltage.
6. Calculate the gain(V_o/V_{in}) and Gain in dB=20log(V_o/V_{in}) ate very frequency.
7. Plot the frequency response curve(taking frequency on X-axis & Gain in dB on Y-axis)using Semi-log Graph.
8. Find out the high cut-off frequency, f_H(at Gain=Constant Gain, A_f–3dB)from the frequency response plotted.
9. Verify the practical(f_H from graph) and the calculated theoretical cut-off frequency ($f_H=1/2\pi RC$).

TABULAR COLUMN:

V_{in}=1V

S .No.	Input Frequency f(Hz)	Output Voltage V_O(V)	Gain Magnitude $\| V_O/V_{in} \|$	Gain in dB= $20\log\| V_O/V_{in} \|$

CALCULATIONS:

THEORETICAL Cut-off frequency:

f_H= 1/ (2πRC)= high cut – off frequency of the Low pass filter.

=

PRACTICAL Cut-off frequency(from Graph):

f_H = high cut-off frequency of the Lowpass filter =3dBcut-offfrequency=

EXPECTEDGRAPH:

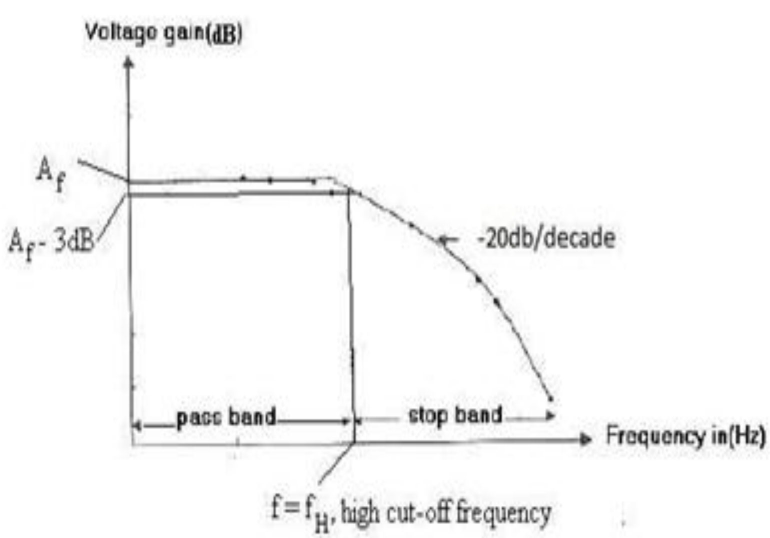


Fig: Active LPF Frequency Response

EXPERIMENTNO:4B

ACTIVE HIGHPASSBUTTERWORTHFILTERS(1st ORDER)

b) 1st Order HIGHPASSFILTER

AIM: To plot the frequency response of Butterworth HPF (First order) and find the low cut-off frequency.

PRELAB:

1. Study the purpose of using Operational amplifiers
2. Learn about Active Filters
3. Identify all the formulae you will need in this Lab.

OBJECTIVES:

After completion of this experiment student will be able to
To Design and setup a Active High Pass Filter using op-amp
To determine the output voltages by providing different R and C values
To plot the frequency response of an integrator circuit

APPARATUS: Bread Board
Function Generator
CRO
Probes
Connecting Wires
741Op-amp, Resistors, Capacitors

THEORY: First Order High Pass Filter consists of RC network for filtering. First Order High Pass filter can be constructed from a First Order Low Pass filter simply by interchangingfrequencydeterminingcomponentsR&C.Op-Ampisusedinthenon–inverting configuration. Resistor $R_1$and $R_F$determine the gain of the Filter. Where $A_F = 1+R_F/R_1$

f=Operating(input)frequency.

f_L=Lowcut-off frequency of the filter.2πRC

.Obviously, all frequencies higher than $f_L$are Pass Band frequencies, with the highest frequency determined by the closed-loop band width of the OP-Amp.

The voltage gain magnitude equation of the second order High-pass filter is

$$\frac{V_0}{V_{in}} = \frac{A_F(f/f_L)}{\sqrt{[1+(f/f_L)^2]}}$$

Where $A_F = 1+R_F/R_1$

f=Operating(input)frequency.

$$f_L = \frac{1}{2\pi RC}$$ =Lowcut-off frequency of the filter.

This is the frequency at which the magnitude of the gain is0.707timesitspassband value. Obviously, all frequencies higher than $f_L$are Pass Band frequencies, with the highest frequency determined by the closed-loop band width of the OP-Amp.

The operation of the high–pass filter can be verified from the gain magnitudeequation.1.Atverylowfrequencies,thatis$f<f_L$

$$|V_o/V_{in}| < A_F$$

2.At $f=f_L$, $|V_o/V_{in}| = A_F/\sqrt{2} = 0.707A_F$

3. At $f>f_L$, $|V_o/V_{in}| = A_F$

For example, in the first order High–Pass filter the gain rolls–of for increases at the rate of 20dB/decade in stop band, that is for input signal frequency lesser than Low cut-offfrequency(f_L);

High Pass filter has constant gain A_F,after the Lowcut-off frequency onwards(f_L).

CIRCUIT DIAGRAM:

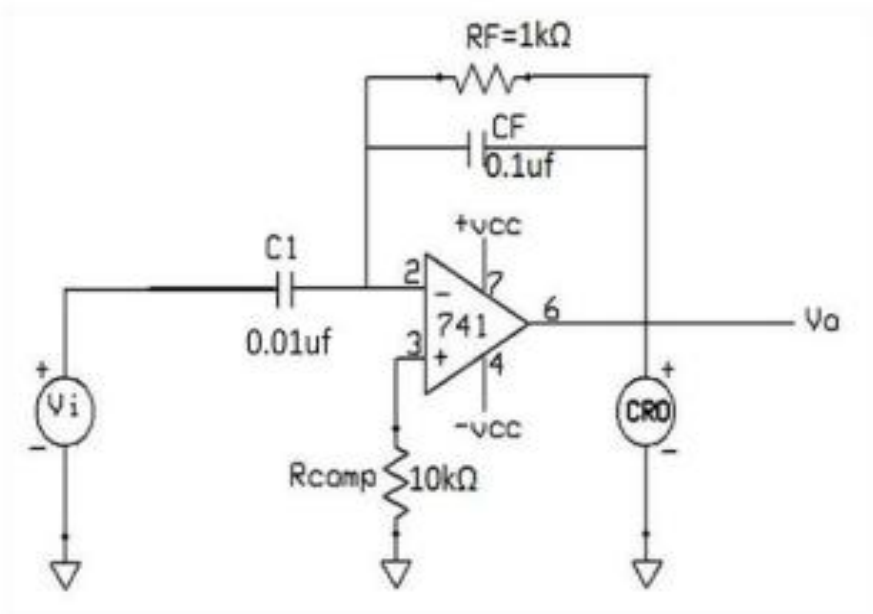


Fig: Differentiator

PROCEDURE:

1. Connect the components/ equipment as shown in the circuit diagram.
2. Switch ON the power supply.
3. Connect channel -1 of CRO to input terminals (V_{in}) and channel -2 to output terminals(V_o).
4. Set V_{in}=1V&f_{in}=10Hzusingfunction generator.
5. By varying the input frequency in regular intervals, note down the output voltage.
6. Calculate the gain(V_o/V_{in}) and Gain in dB=20log(V_o/V_{in})at every frequency.
7. Plot the frequency response curve(taking frequency on X – axis & Gain in dB on Y-axis)using Semi log Graph.
8. Find out the low cut-off frequency, f_L(at Gain=Constant Gain, A_f–3dB)from thefrequency response plotted.
9. Verify the practical (f_L from graph) and the calculated theoretical cut-off frequency ($f_L = 1/2\pi RC$

TABLUAR COLUMN:

V_{in}=1V

S.No.	Input Frequency f(Hz)	Output Voltage Vo(V)	Gain Magnitude | Vo/Vin|	Gain in dB= 20log| Vo/Vin|

CALCULATIONS:

THEORETICAL Cut-off frequency:

f_L= 1/(2πRC)=Low cut-off frequency of the HPF.

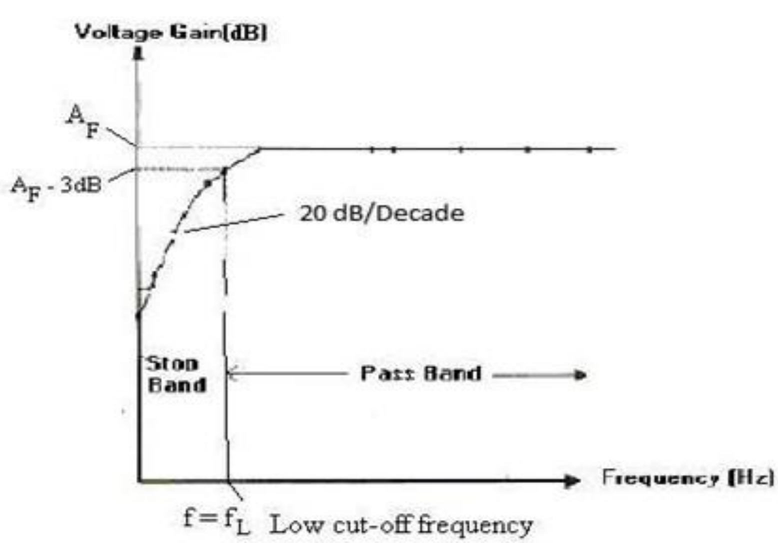
=

PRACTICAL Cut-off frequency:

f_L = Low cut-off frequency of the HPF. = 3dBcut-off frequency

=

EXPECTEDGRAPH:



RESULT: The frequency response of lpf & hpf (1st order)had plotted

Viva Question's:

1. How filters are classified ? Give one example for each classification.
2. What is an active filter and why it is called so?
3. How an active filter differs from a passive filter?
4. What are the advantages of active filters over passive filters?
5. Draw the circuit diagrams of active filters LPF and HPF.
6. Draw the frequency response of all filters(LPF, HPF, BPF, BRF and All-pass).
7. Whatisthegainrolloffratefora1st order and 2nd order filter?
8. What is the formula for cut-off frequency?
9. What is a 3dB frequency and why it is called so?
10. What are the other names for 3db frequency?
11. Formula for the gain of inverting amplifier?
12. Formula for the gain of non-inverting amplifier?
13. Define op-amp?
14. Difference between closed loop and open loop feedback?
15. Difference between inverting amplifier op-amp and non-op-amp
16. Draw the circuit of the integrator using op-amp?
17. Draw the frequency response of the integrator?
18. Define slew rate?
19. Define CMRR?
20. Define low pass filter?
21. What output does comparator generates when Vin>Vref?
22. What are the real time applications of comparator?
23. How many input parameters are required for comparator?
24. Draw the circuit of inverting & non-inverting comparator?
25. What are the differences between inverting & non - inverting?
26. Define Comparator?
27. What is the gain of non-inverting op-amp?
28. What is the gain of inverting op-amp?
29. What are linear applications of op-amp?
30. What are non-linear applications of op-amp?
31. What are applications of open loop configuration?
32. What are the characteristics of differential amplifier?
33. Why comparator is called voltage level detector?
34. What is the name of comparatorifreferencevoltageis0V?
35. What is formulae for gain of amplifier?
36. What is formulae for output voltage of differential amplifier?
37. Formula for the gain of inverting amplifier?
38. Formula for the gain of non-inverting amplifier?
39. Define op-amp?
40. Difference between closed loop and open loop feedback?
41. Difference between inverting amplifier op-amp and non-op-amp
42. Draw the circuit of the integrator using op-amp?
43. Draw the frequency response of the integrator?

44. What is the output of subtractor if V1=1v&V2=3v?
45. What is negative feedback in op-amp?
46. What is positive feedback in op-amp?
47. What is open loop configuration of op-amp?
48. What is closed loop configuration of op-amp?
49. What are the DC characteristics of op-amp?

REAL TIME APPLICATIONS

Active filters applications- LPF HPF

Active Low Pass Filters are used in audio amplifiers, equalizers or speaker systems to direct the lower frequency bass signals to the larger bass speakers or to reduce any high frequency noise or “hiss” type distortion. When used like this in audio applications the active low pass filter is sometimes called a “Bass Boost” filter.

Active High Pass Filters are in audio amplifiers, equalizers or speaker systems to direct the high frequency signals to the smaller tweeter speakers or to reduce any low frequency noise or “rumble” type distortion. When used like this in audio applications the active high pass filter is sometimes called a “Treble Boost” filter.

EXPERIMENTNO:5 DATE:

IC741WAVEFORM GENERATORS–SINE,SQUARE WAVE AND TRIANGULAR WAVES

AIM: To design a Waveform Generator which generates Sine, Square and Triangular wave forms using IC741 and to verify it's various output waveforms.

PRELAB:

1. Study the purpose of using Operational amplifier IC 741
2. Learn about Waveform generators such as Oscillators, Multivibrators
3. Identify all the formulae you will need in this Lab.

OBJECTIVES:

After completion of this experiment student will be able to
To Design and setup a Sine wave generator using op-amp
To Ddetermine the output voltages by providing different R and C values
To plot the waveforms of different wave generators

APPARATUS: BreadBoard
CRO
Probes
741Op-amp, Resistors, Capacitors

THEORY:

Waveform generator using IC741 is a circuit which generates Sine wave, square wave and Triangular wave. This circuit is a combination of Wien Bridge oscillator, zero crossing detector (Comparator with zero reference voltage) and Integrator. The Wien Bridge oscillator generates Sine wave which is fed to the input of Zero crossing detector. This detector gives the square wave output which's connected to the input of the Integrator which in turn produces the Triangular wave output.

The frequency of oscillations of the Sine wave output of Wien Bridge oscillator is given by $f_O=1/2\pi RC$

The frequency of oscillations of Square and Triangular wave outputs will also be the same frequency as that of the Sine wave output.

For theory of individual circuits i.e. Wien Bridge oscillator, Zero Crossing Detector and Integrator, please refer to the THEORY section of respective experiments mentioned earlier in this manual.

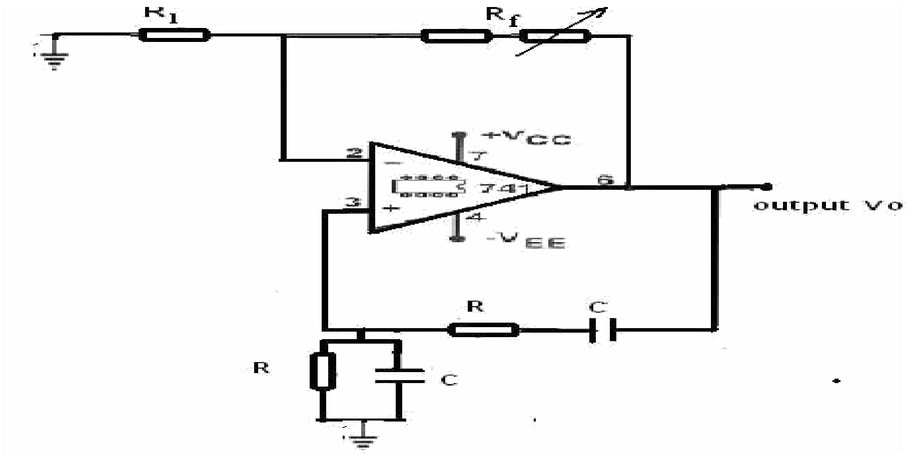
DESIGN for Wien Bridge Oscillator:

1. Choose a desired frequency of oscillation, say f_O=500Hz.

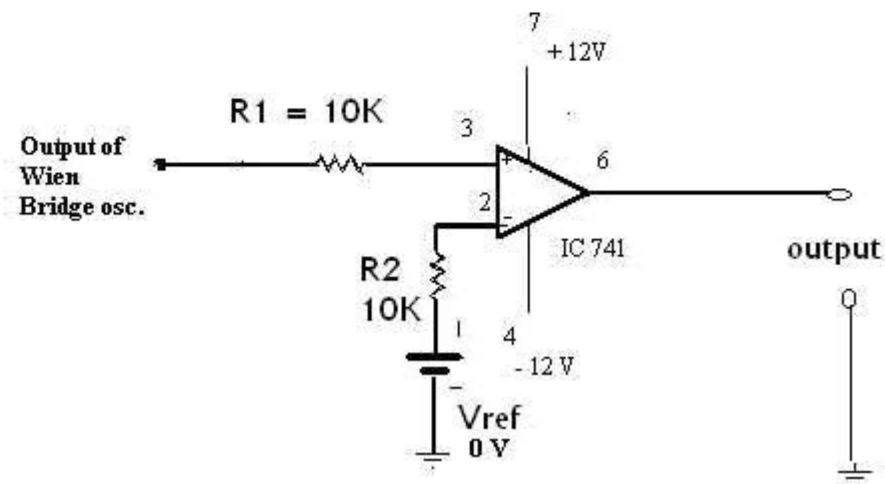
2. Choose a value for capacitor C(0.1 μF) and then calculate the value of R by using the equation for f_o(f_o=1/2πRC).
3. Choose a value for R_1 (10 KΩ) and calculate the value of R_f from the gain equation(A_V = 1+R_f/R_1 = 3). (Note: In practical, the value of R_f may need to be varied to bemore than the calculated value.)

CIRCUITDIAGRAM:

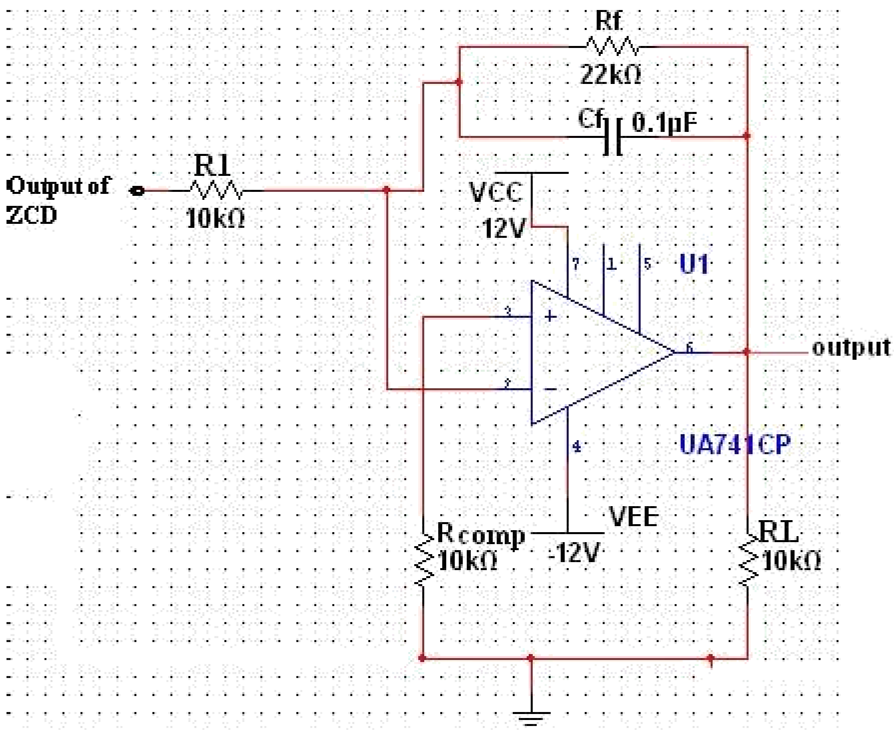
Sine Wave Generator (Wien Bridge Oscillator):



Square Wave Generator (Zero Crossing Detector):



Triangular Wave Generator (Integrator):



PROCEDURE:

Sine wave Generator:

1. Connect the components/equipment as shown in the circuit diagram.
2. Switch ON the power supply.
3. Connect output to the CRO.
4. Adjust the potentiometer to get an undistorted waveform.
5. Note down the amplitude and the time period, T of the sine wave and calculate the frequency of oscillation, $f_O=1/T$.
6. Verify the practical frequency of oscillation calculated in the preceding step with the theoretical value, $f_O=1/2\pi RC$.
7. Plot the waveform.

Square wave Generator:

1. Switch OFF the power supply.
2. Connect the components/equipment as shown in the circuit diagram.
3. Switch ON the power supply.
4. Connect the input to the channel-1 of CRO and output to the channel-2 of CRO.

5. Observe the square wave output at channel-2 and note down the amplitude and time period, T of the waveform.
6. Verify that the frequency of oscillation of both the input and the output wave sis same. Also verify that both the input and the output waves are in same phase. Plot the output wave form in accordance with the

Triangular wave Generator:

1. Switch OFF the power supply.
2. Connect the components/equipment as shown in the circuit diagram.
3. Switch ON the power supply.
4. Connect the input to the channel-1of CRO and output to the channel-2of CRO.
5. Observe the triangular wave output at channel-2 and noted own the amplitude and time period, T of the waveform.
6. Verify that the frequency of oscillation of both the input and the output waves is same. Also verify that the output wave is inverted i.e.180^ophase shift from the input wave.
7. Plot the output waveform in accordance with the input waveform.
7. input waveform

CALCULATIONS:

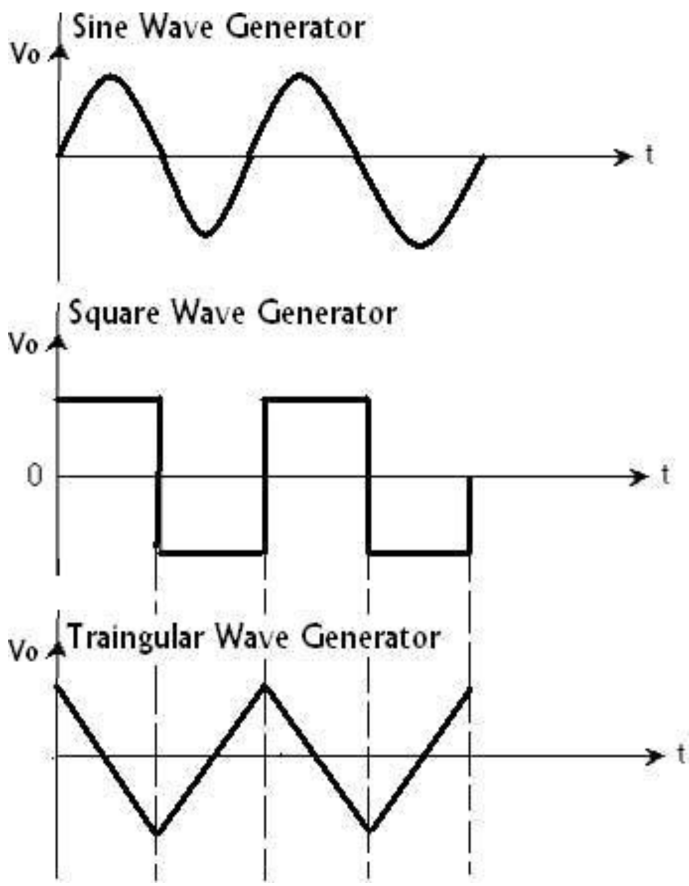
THEORETICAL Frequency of Oscillation $f_O = 1/2\pi RC$

=

PRACTICAL Frequency of Oscillation $f_O = 1/T$

=

EXPECTEDWAVEFORMS:



RESULT: The Waveform Generator which generates Sine, Square and Triangular wave forms using IC741 and to verify it's various output waveforms.

Viva Question's

1. What is a Function Generator?
2. What are the different stages in a Function Generator and how they are connected?
3. Draw the output wave forms at different stages of Function Generator.
4. What is the relationship among the frequencies of output waveforms at different stages of Function Generator?
5. Will there be any phase shift between the input and the output of any stage in the Function Generator and what factor it depends on?
6. Why is R_{comp} used in the circuit of Triangular wave generator?
7. Why is potentiometer used in the circuit of Wien Bridge Oscillator?
8. Formula for the gain of inverting amplifier?
9. Formula for the gain of non-inverting amplifier?
10. Define op-amp?
11. Difference between closed loop and open loop feed back?
12. Difference between inverting amplifier op-amp and non-op-amp
13. Draw the circuit of the integrator using op-amp?
14. Draw the frequency response of the integrator?
15. Define slew rate?
16. Define CMRR?
17. What output does comparator generates when Vin>Vref?
18. What is meant by clipper circuit?
19. What is the 'tilt' applicable to RC circuits ? Give an expression for tilt?
20. What type of distortion is observed in monostable multivibrator?
21. What is meant by clamper circuit?
22. Give two applications of Schmitt Trigger circuit...?
23. Why do we call monostable multivibrator as free running multivibrator?
24. Define the threshold points in a Schmitt trigger circuit.?
25. What is are generative comparator?
26. Distinguish between symmetrical and unsymmetrical triggering methods
27. A monostable 555 timer has the following number of stable states?
28. The mono stable multivibrator circuit is not an oscillator because_.?
29. To obtain a 50% duty cycle in an monostable 555 timer circuit?
30. How many stable states are present in monostable 555 timer?
31. Which of the following is NOT a characteristic of a re triggerable monostable multivibrator?
32. What does the monostable do?
33. What is the main purpose of monostable multivibrator?
34. What is the other name of monostable multivibrator?
35. Disadvantages of monostable multivibrator?
36. Monostable multivibrator is used as ?
37. What type of transistors are used in monostable multivibrator?
38. Monostable multivibrator has a?

39. Characteristics of retrigger able monostable multivibrator?
40. Block diagram of monostable multivibrator?
41. Draw the circuit of the Differentiator using op-amp IC741.
42. Write down the expression for VO of a Differentiator.
43. Difference between closed loop and open loop feedback?
44. Difference between inverting amplifier op-amp and non-op-amp
45. Draw the circuit of the integrator using op-amp?
46. Draw the frequency response of the integrator?

REAL TIME APPLICATIONS

IC741 waveform generators applications

1. The operational amplifier based square waveform generator is a simple circuit that is widely used in function generators.

The operational amplifier based square waveform generator is a simple circuit that is widely used in communication systems

EXPERIMENTNO:6 DATE

MONOSTABLEMULTIVIBRATOR USING IC555

AIM: To design a Monostable Multivibrator using IC555 and compare it's theoretical and practical pulse width.

PRELAB:

1. Study the purpose of using IC 555 Timer
2. Learn about different Multivibrators
3. Identify all the formulae you will need in this Lab.

OBJECTIVES:

After completion of this experiment student will be able to
To Design and setup a Monostable Multivibrator using IC 555
To determine the Time period
To plot waveforms of Monostable Multivibrator

APPARATUS:

Bread Board.
CRO
Probes
Connecting wires
Resistors, Capacitors
IC 555 Timer

THEORY:

Monostable multivibrator is also called as one–shot Multivibrator. When the output is low, the circuit is in stable state, transistor T1 is ON and Capacitor C is shorted to the ground. However, upon application of a negative trigger pulse to Pin–2, transistor T1 is turned OFF, which releasesshortcircuitacrosstheexternalcapacitoranddrivestheoutputHigh.The capacitor C now starts charging up toward V_{CC} through R. However when the voltage across the external capacitor equals 2/3 V_{CC}, upper comparator's output switches from low to high which inturn derives the output to its low state. And the output of the flip flop turns transistor T1 ON, and hence the capacitor C rapidly discharges through the transistor. The output of the Monostable remains low until a trigger pulse is a gain applied. Then the cycle repeats. The time during which the output remains high is given by

$$t_p=1.1RC$$

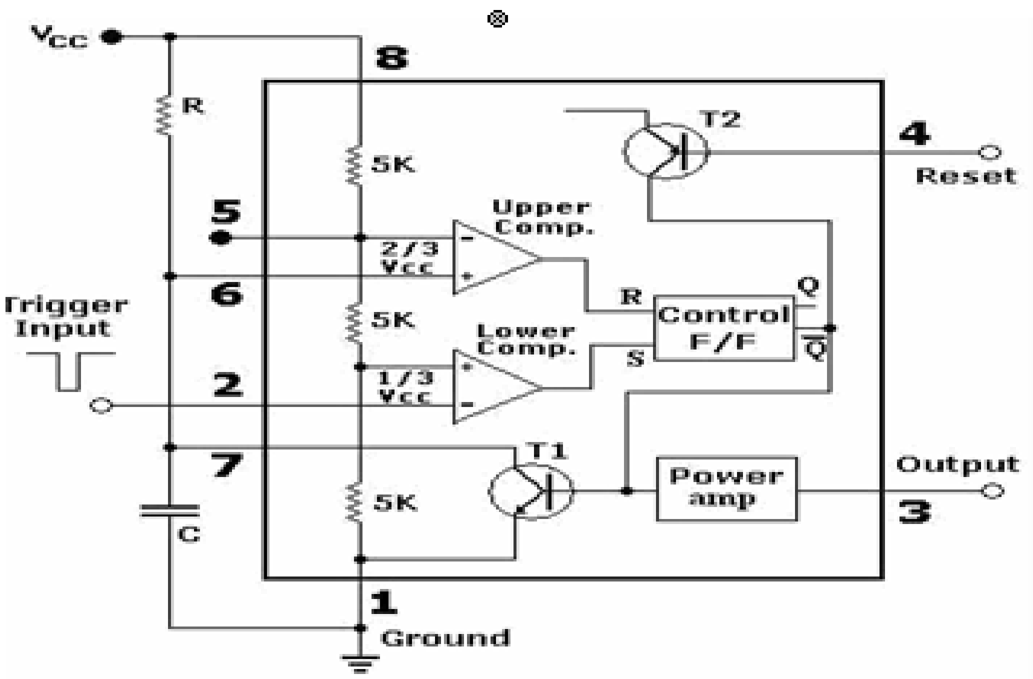


Fig: Internal Circuit Diagram of IC555MonostableMultivibrator

Once triggered, the circuit's output will remain in the high state until the set time t_p elapses. The output will not change its state even if an input trigger is applied again during this time interval t_p.

.

CIRCUITDIAGRAM:

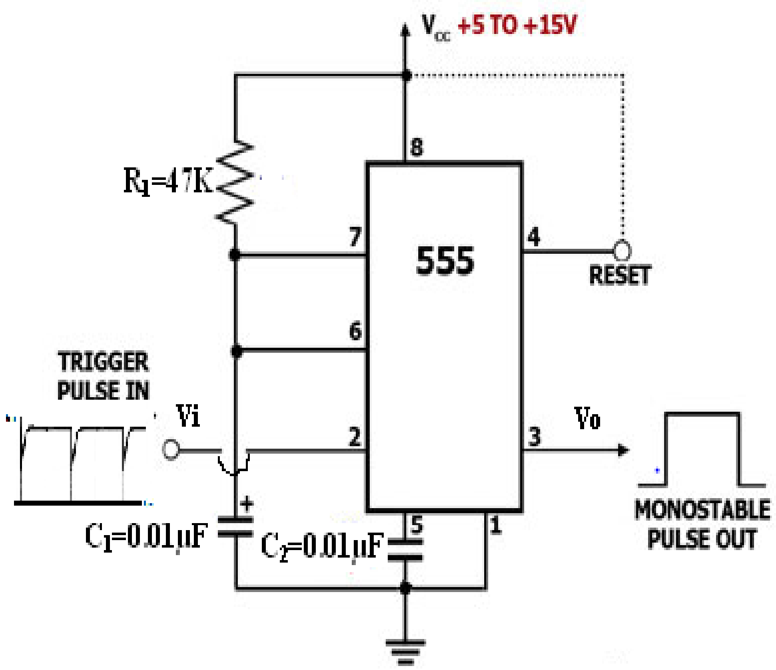


Fig: IC555 Monostable Multivibrator

PROCEDURE:

1. Connect the components/equipment as shown in the circuit diagram.
2. Switch ON the power supply.
3. Connect function generator at the trigger input.
4. Connect channel-1of CRO to the trigger input and channel-2 of CRO to the output(Pin3).
5. Using Function Generator, apply 1KHz square wave with amplitude of approx. equal to 9Vpp at the trigger input.
6. Observe the output voltage with respect to input and note down the pulse width and amplitude.
7. Now connect channel-2 of CRO across capacitor and observe the voltage across

the capacitor and note it down.

8. Compare the practical pulse width noted in the step above with its theoretical value (t_p=1.1RC)

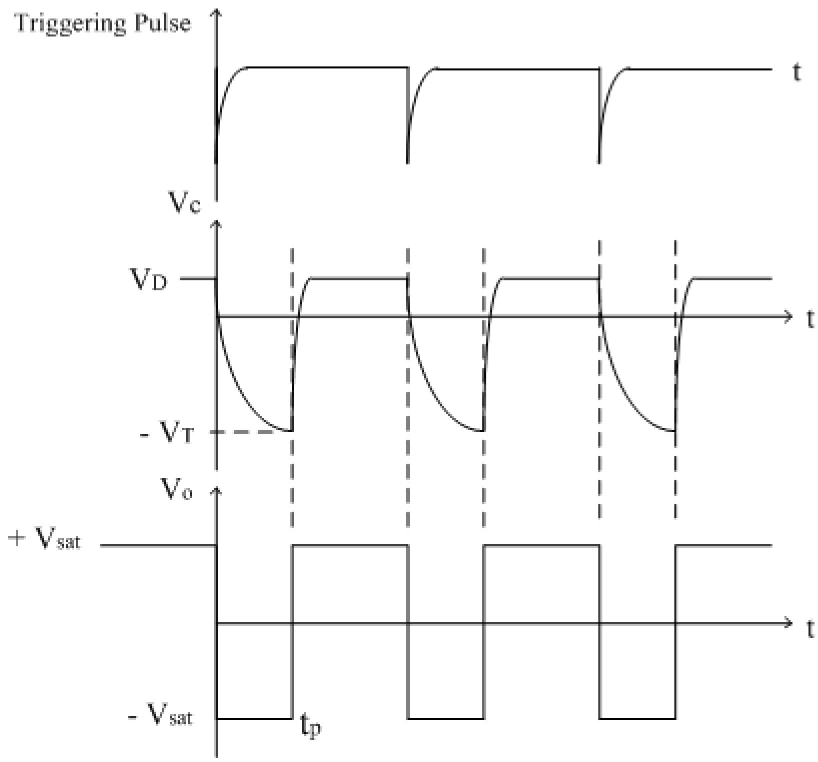
CALCULATIONS:

THEORETICAL

Pulse width R= C=

t_p=1.1RC =PRACTICAL Pulse width t_p=

EXPECTED WAVEFORM



RESULT: Monostable Multivibrator using IC555 and compare it's theoretical and practical pulse width.

Viva Question's

1. What is the other name for monostable multivibrator (MSMV)?
2. When MSMV is in stable state, what is the output level?
3. Why trigger is required in the case of MSMV ?
4. Which type of trigger pulse is required for MSMV ?
5. What is the formula for the output pulse width of MSMV?
6. How long MSMV stays in unstable state?
7. Multivibrators belong to a family of oscillators commonly called?
8. Circuit which consists of a quasi-stable state is called?
9. Capacitor discharge interval in monostable circuits is known as?
10. What is the main use of monostable multivibrator?
11. Astable vibrator contains?
12. Determine the time period of a monostable 555 multivibrator?
13. Find monostable vibrator circuit using 555timers?
14. How to overcome is triggering on the positive pulse edges in the monostable circuit?
15. A monostable multivibrator has R = 120kΩ and the time delay T = 1000ms, calculate the value of C?
16. Which among the following can be used to detect the missing heartbeat?
17. A 555timer in monostable application mode can be used for?
18. How can a monostable multivibrator be modified into a linear ramp generator? Determine time period of linear ramp generator using the specifications R_E= 2.7kΩ,R_1=47kΩ,R_2 100kΩ,C= 0.1µF,V_{CC}=5v.?
19. Advantages of monostable multivibrator?
20. Give two applications of monostable multivibrators?
21. How does a diode act as a comparator?
22. What is meant by clipper circuit?
23. What is the 'tilt 'applicable to RC circuits ?Give an expression for title?
24. What type of distortion is observed in monostable multivibrator?
25. What is meant by clamper circuit?
26. Give two applications of Schmitt Trigger circuit...?
27. Why do we call monostable multivibrator as free running multivibrator?
28. Define the threshold points in a Schmitt trigger circuit.?
29. What is a regenerative comparator?
30. Distinguish between symmetrical and unsymmetrical triggering methods.?
31. Why Monostable multivibrator is also called as delay circuit?
32. What is the function of the comparators in the 555-timer circuit?
33. When the capacitor charges to the source voltage ?
34. The_is defined as the time the output is active divided by the total period of the output signal.

35. A22-k Ωresistor and a 0.02- F μcapacitor is connected in series to a 5-V source. How long will it take the capacitor to charge to 3.4V?
36. What does the discharge transistor do in the 555-timer circuit?
37. With most monostable multivibrators , what is the *Q* output when no input trigger has occurred ?
38. The monostable multivibrator requires :
39. What is the difference between an astable multivibrator and a monostable multivibrator?
40. The output of the monostable circuit_.?
41. In a typical IC monostable multivibrator circuit, at the falling edge of the trigger input, the output switches HIGH for a period of time determined by the_.?
42. A 555 timer in monostable application mode can be used for?
43. How can a monostable multivibrator be modified into a linear ramp generator?
44. Determine time period of linear ramp generator using the specifications RE= 2.7kΩ, R1=47kΩ, R2 100kΩ, C= 0.1μF, VCC=5v.?
45. List of advantages of monostable multivibrator?
46. Give two applications of monostable multivibrators?
47. How does a diode act as a comparator?
48. Why do we have to give positive feedback for a Schmitt trigger?
49. What are the conditions to get a perfect square wave from the Schmitt trigger?

REAL TIME APPLICATIONS

The various applications of Monostable Multivibrator Using IC 555 are,

1. Frequency divider.
2. Pulse width modulation.
3. Linear ramp generator.
4. Pulse position modulation.
5. Missing pulse detector.
6. Timer in relay

EXPERIMENT No:7 DATE

THREETERMINALVOLTAGE REGULATORS–7805,7809,7912

AIM

To study the Fixed Voltage Regulators(1)7805
(2)7809
(3)7812

PRELAB:

1. Study the purpose of using Voltage Regulators
2. Learn about different IC Voltage Regulators
3. Identify **7805,7809,7912** Voltage Regulators
4. Plot Line and lo

OBJECTIVES:

Theory

DC power for electronic circuits is most conveniently obtained from commercial ac lines by using rectifier - filter system, called a dc power supply. The rectifier-filter combination constitutes an ordinary dc power supply . The dc voltage from an ordinary power supply remains constant so long as ac mains voltage or load is unaltered. However, in many electronic applications, it is desired that Constant Dc voltage should remain irrespective of changes in ac mains or load. Under such situations, voltage regulating devices are used with ordinary power supply. This constitutes regulated dc power supply and keeps the dc voltage at fairly constant value.

ORDINARY DC POWER SUPPLY

An ordinary or regulated dc power supply contains a rectifier and a filter circuit as shown in Fig-1. The output from the rectifier is pulsating dc. These pulsations are due to the presence of ac component int he rectifier output. The filter circuit removes the ac component so that steady dc voltage is obtained across the load.

Limitations : An ordinary dc power supply has two following drawbacks:1.The dc output voltage changes directly with input ac voltage.

2. The dc output voltage decreases as the load current increases. This is due to voltage drop in(a)Transformer windings(b)Rectifier(c)Filter circuit

These variations in dc output voltage may cause in accurate or erratic operation or even malfunctioning of many electronic circuits.

REGULATED POWER SUPPLY

A dc power supply which maintains the output voltage constant irrespective of ac mains fluctuations or load variations is known as regulated dc power supply. A regulated power supply consists of an ordinary power supply and voltage regulating device an in fig-4. The output of ordinary power supply is fed to the voltage regulator which produces the final output. The output voltage (Vdc) remains constant whether the load current changes or there are fluctuations in the input ac voltage.

HARDWARESPECIFICATIONS

1. Built-in16V -0-16V/350mA
   12V -0-12V/350mA
   8V-0-8V/350mA AC sources
2. Bridge rectifier usingIN4007 diodes-1No.
3. Filter capacitors(470□F/ 35V) -2Nos.
4. Fixed Voltage Regulator 7805-1No.
   7809-1No.
   7812-1No.
   7912-1No.
5. Variable Voltage Regulator using 723IC

EXPERIMENTAL PROCEDURE

1. Connect the circuit as shown in fig-4.
2. Connect different load resistors available in the front panel, note down the output current and voltage.
3. Also test the circuit with12V-0-12V,16V -0-16VAC sources also.
4. Remove 7805 and connect 7809,7812 also repeat 2 and 3 steps.
5. Connect the circuit shown in fig-5.

EXPERIMENT-8

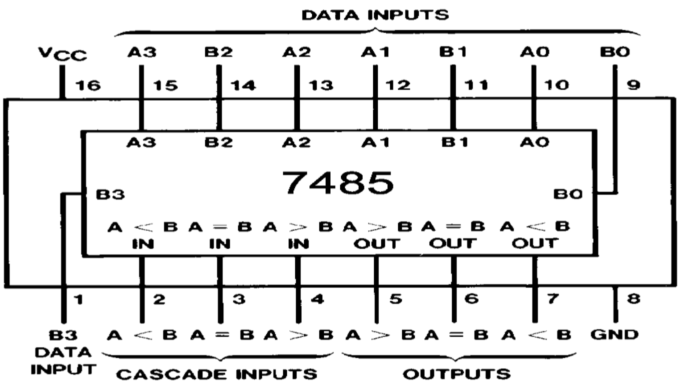
16-BITCOMPARATORUSING4BITCOMPARATORS

AIM:
Toconstructandverifya16Bit Comparatorusing4 Bit Comparators.

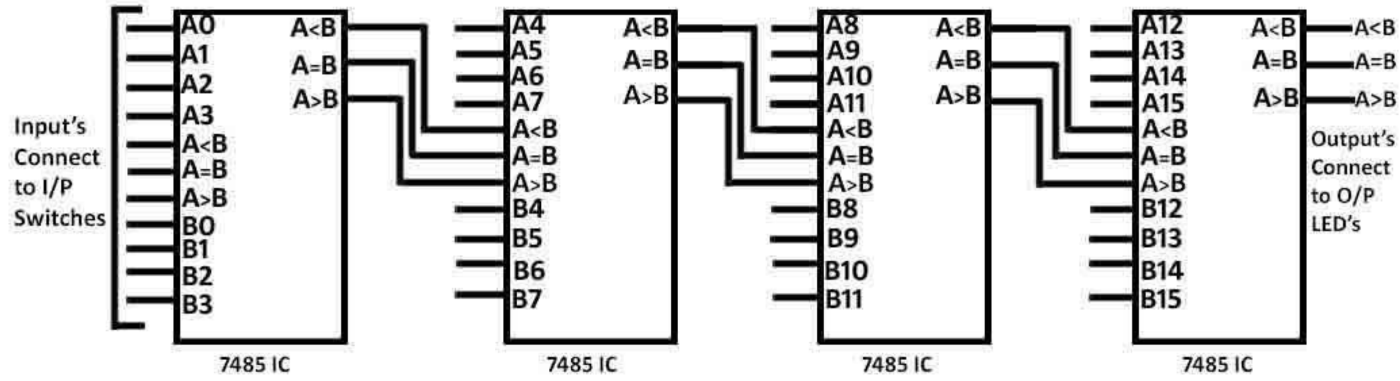
APPARATUS:
1. 16Bitcomparatorusing4 Bit comparator trainer kit.
2. Patch cords.

THEORY:
Data comparison is needed in digital systems while performing arithmetic or logical operations. This comparison determines whether one number is greater than, equal, or less than the other number. A digital comparator is widely used in combinational system and is specially designed to compare the relative magnitudes of binary numbers. These are also available in IC form with different bit comparing configurations such as 4-bit, 8-bit, etc. More than one comparator can also be connected in cascade arrangement to perform comparison of numbers of longer lengths. Whenever we want to compare the two binary numbers, first we have to compare the most significant bits. If these MSBs are equal, then only we need to compare the next significant bits. But if the MSBs are not equal, then it would be clear that either A is greater than or less than B and the process of comparison ceases. For example, the two 2-bit number are A= A1A0 and B=B1B0. If A1 is not equal to B1, then it is clear that A is greater than B for A1=1 & B1=0 or else A is less than B for A0=0 & B0=1. At this stage the process of comparison ceases. If the MSBs are equal, i.e., A1=B1, only then we need to compare the next significant bits A0 and B0 and decide whether the number is greater than, less than or equal. So, the comparator produces three outputs as L, E and G corresponds to less than, equal and greater than comparisons. A magnitude digital comparator is a combinational circuit that compares two digital or binary numbers (consider A and B) and determines their relative magnitudes in order to find out whether one number is equal, less than or greater than the other digital number. Three binary variables are used to indicate the outcome of the comparison as A>B, A<B, or A=B. The below figure shows the block diagram of an n-bit comparator which compares the two numbers of n-bit length and generates their relation between themselves. These comparators can compare 2-bit, 4-bit, and 8-bit numbers depending on the application requirement.

PINCONFIGURATION:



CIRCUITDIAGRAM:



PROCEDURE:

1. Connect the circuit as shown in circuit Diagram.
2. Connect the Comparing Inputs to the Input switches, which are present on the trainer kit.
3. Connect the Cascading Inputs to the Input switches, which are present on the trainer kit.
4. Connect Outputs to the LED's.
5. Observe output and verify with the truth table as given below.

TRUTH TABLE:

NOTE: Connect Cascading Inputs to the Input switches and apply the condition for all below given table **A<B–L, A=B–H,A>B–L.**

COMPARINGINPUTSA0toA15																COMPARINGINPUTSB0toB15																OUTPU		
A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A1	A1	A1	A1	A1	A1	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B1	B1	B1	B1	B1	B1	A>	A=	A<
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

RESULT: -

The 16Bit Comparator using4 Bit Comparators was designed and implemented.

VIVA QUESTIONS:

1. What is Magnitude Comparator?
2. List out the applications of comparators?
3. What is digital comparator?
4. Realize a single bit comparator?
5. Which logic gate is a basic comparator?
6. When are two numbers are equal?
7. What are the different types of comparators?
8. What are the advantages of comparator?
9. If two numbers are not equal then binary variable will be
10. A procedure that specifies finite set of steps is called?
11. How many 4-bit comparators are needed to construct 12-bit comparator?
12. What does a digital comparator mean?
13. Design a 2-bit comparator using gates?
14. Explain the phases of a simulation?
15. Explain briefly about wait statement?
16. What do you mean by Logic Gates?
17. What are the applications of Logic Gates?
18. What is Truth Table?
19. Why we use basic logic gates?
20. Write down the truth table of all logic gates?
21. What do you mean by universal gate?
22. Write truth table for 2 input NOR, NAND gate?

23. Implement all logic gate by using universal gate?

24.Why is they called universal Gates?

25. Give the name of universal gate?

26. Draw the circuit diagram of Half adder circuit?

27.Draw the circuit diagram of full adder circuit?

28 Draw the full adder circuit by using Half Adder circuit and minimum no. of logic gate?

29.Write Boolean function for half adder?

30. Write Boolean function for Full adder?

31.Design the half Adder and Full adder using NAND-NAND Logic.

32. Draw the circuit diagram of Half Subtractor circuit?

33.Draw the circuit diagram of full subtractor circuit?

34.Draw the full subtractor circuit by using half subtractor circuit and minimum no. of logic gate?

35. Write Boolean function for half 7ubtractor?

36.Write Boolean function for Full Subtractor?

37. What is Excess-3 code? Why it is called Excess-3 code?

38.What is the application of Excess-3 code?

39. What is ASCII code?

40. Excess-3 code is Weighted or Unweighted?

41.Out of the possible 16 code combination? How many numbers used in Excess-3 code?

42.Which logic gate is a basic comparator?

43.When are two numbers are equal?

44.What are the different types of comparators?

45.What are the advantages of comparator?

46.If two numbers are not equal then binary variable will be

47.A procedure that specifies finite set of steps is called

48.How many 4-bit comparators are needed to construct 12-bit comparator?

49. What does a digital comparator mean?

50. Design a 4-bit comparator using gates?

EXPERIMENT-9

A450KHzCLOCKUSINGNAND/NORGATES

AIM:

To study the Clock Generation by using NAND Gate and NOR Gate.

APPARATUS:

1. Clock Generator using NAND/NOR Gates Trainer kit
2. Patch Cords

THEORY:

Schmitt Waveform Generators can also be made using standard CMOS Logic NAND/NOR Gates connected to produce an inverter circuit. Here, two NAND/NOR gates are connected together to produce another type of RC relaxation oscillator circuit that will generate a square wave-shaped output waveform as shown in the circuit diagram.

In this type of waveform generator circuit, the RC network is formed from resistor, R1 and the capacitor, C with this RC network being controlled by the output of the first NAND/NOR gate. The output from this R1C network is fed back to the input of the first NAND/NOR gate via resistor, R2 and when the charging voltage across the capacitor reaches the upper threshold level of the first NAND/NOR gate, the NAND/NOR gate changes state causing the second NAND/NOR gate to follow it, thereby change state and producing a change in the output level.

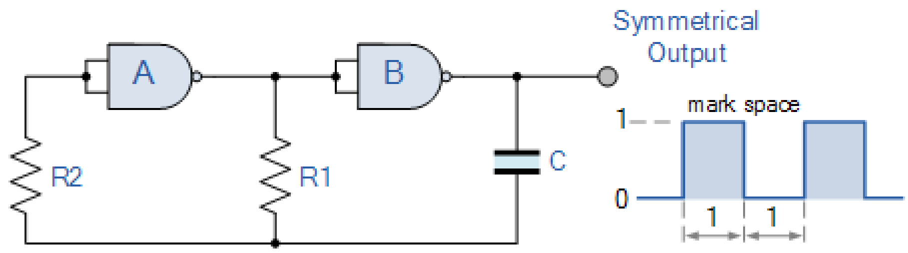
The voltage across the R1C network is now reversed and the capacitor begins to discharge through the resistor until it reaches the lower threshold level of the first NAND/NOR gate causing the two gates to change state once again. Like the previous Schmitt waveform generators circuit above, the frequency of oscillation is determined by the R1C time constant which is given as: 1/2.2R1C. Generally, R2 is given a value that is 10 times the value of resistor R1. When high stability or guaranteed self-starting is required, CMOS Waveform Generators can be made using three inverting NAND/NOR gates or any three logic inverters for that matter, connected together as shown below producing a circuit that is sometimes called “the ring of three” of three-waveform generator. The frequency of oscillation is determined again by the R1C time constant, the same as for the two-gate oscillator above, and which is given as: 1/2.2R1C when R2 has a value that is 10 times the value of resistor, R1.

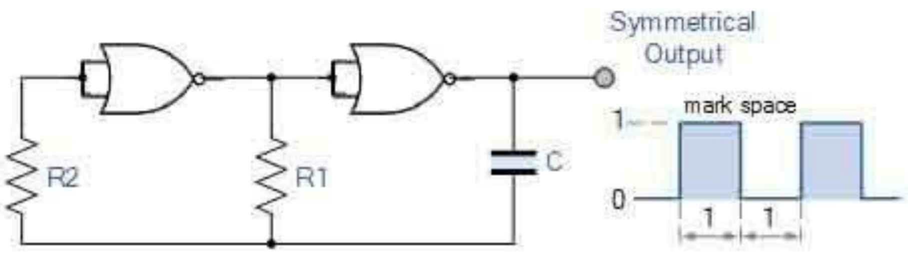
The addition of the extra NAND/NOR gate guarantees that the oscillator will start even with very low capacitor values. Also, the stability of the waveform generator is greatly improved as it is less susceptible to power supply variations due to its threshold triggering level being nearly half of the supply voltage. The amount of stability is mainly determined by the frequency of oscillation and generally speaking, the lower the frequency the more stable the oscillator becomes.

As this type of waveform generator operates at nearly half or 50% of the supply voltage, the resultant output waveform has very nearly a 50% duty cycle, 1:1 mark-space ratio. The three-gate waveform generator has many advantages over the previous two-gate oscillator above but its one big disadvantage is that it uses an additional logic gate

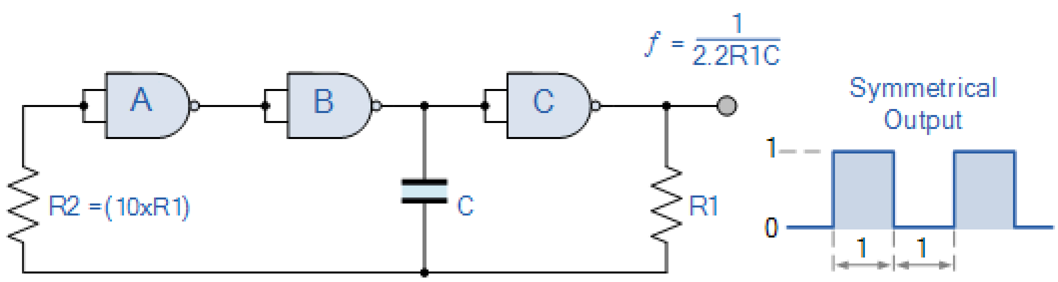
CIRCUIT DIAGRAM:

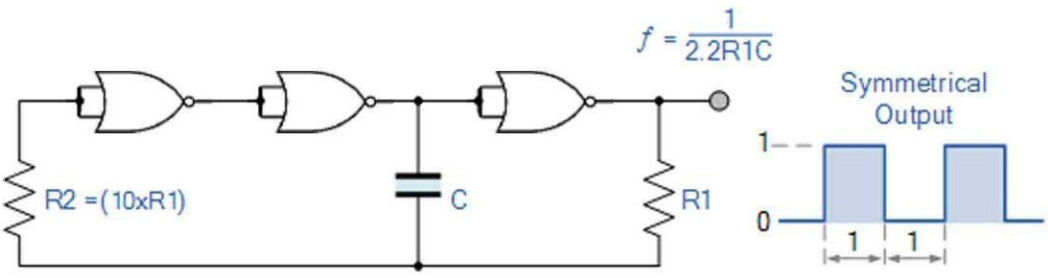
NAND/NOR Gate Waveform Generator:





Stable NAND/NOR Gate Waveform Generator:





PROCEDURE:

1. Switch ON the Clock Generator using NAND/NOR Gates trainer kit.
2. Connect the any Resistor which are present on the trainer kit to **R** terminal in NAND/NOR Gate circuit.
3. Connect the any Capacitor which are present on the trainer kit to **C** terminal in NAND/NOR Gate circuit.
4. Connect CRO/DSO Channel 1to the Clock O/P of NAND/NOR Gate.
5. Observe the O/P wave form and Frequency by varying the Resistor (R) and Capacitor (C) Values.

RESULT:
The Clock Generation by using NAND Gate and NOR Gate was studied.

VIVA QUESTIONS:

1.What are the universal gates? Why they are called so?

2.Realize the EX – OR gates using minimum number of NAND gates.

3. Give the truth table for EX-NOR and realize using NAND gates?

4.What are the logic low and High levels of TTL IC's and CMOS IC's?

5. Compare TTL logic family with CMOS family?

6. Which logic family is fastest and which has low power dissipation?

7.What are the different methods to obtain minimal expression?

8.What is a Min term and Max term

9.State the difference between SOP and POS.

10. What is K-map? Why is it used?

11.What do you mean by Logic Gates?

12.What are the applications of Logic Gates?

13.What is Truth Table?

14. Why we use basic logic gates?

15.Write down the truth table of all logic gates?

16.What do you mean by universal gate?

17.Write truth table for 2 input NOR, NAND gate?

18. Implement all logic gate by using universal gate?

19.Why is they called universal Gates?

20. Give the name of universal gate?

21. Draw the circuit diagram of Half adder circuit?

22.Draw the circuit diagram of full adder circuit?

23 Draw the full adder circuit by using Half Adder circuit and minimum no. of logic gate?

24.Write Boolean function for half adder?

25. Write Boolean function for Full adder? 261. Design the half Adder and Full adder using NAND-NAND Logic.

26.Pseudo Random Sequence Generator also known as what?

27.Ring counter belong to which type of counter?

28.What are the types of ring counter?

29. What is the difference between Johnson Ring Counter and synchronous ring counter?

30.What is meant by pseudo random number generator?

31. List out the applications of PRNG.

32. TRNG stands for

33. Define Uniformity in PRNG

34. Define scalability.

35. Write the syntax for component declaration.

36. Write the behavioral code for IC 74x189 without declaring the function

37. Explain about different types of RAMs?

38. How to specify the memory size?

39. Explain read and write operations?

40. What are the differences between RAM and RAM?

41. Explain the steps of a compilation process of a VHDL program?

42. Explain the types of design units?

43. Why configurations are needed?

44. What is binding?10. What is subprogram in VHDL

45.Write the behavioral code for the IC 74x74.

46. Write the dataflow code for the IC 74x74.

47. What is the difference between sequential and combinational circuit?

48. What is a flip-flop? Explain the functions of preset and clear inputs in flip-flop?

49. What is meant by a clocked flip-flop?

50. What is meant by excitation table?

EXPERIMENT-10

4 BIT PSEUDO RANDOM SEQUENCE GENERATOR USING 4 BIT RING COUNTER

AIM:
To construct and study the Pseudo Random Sequence Generator using Ring Counter

APPARATUS:

1. Pseudo Random Sequence Generator using Ring Counter trainer kit
2. Patch Cords.

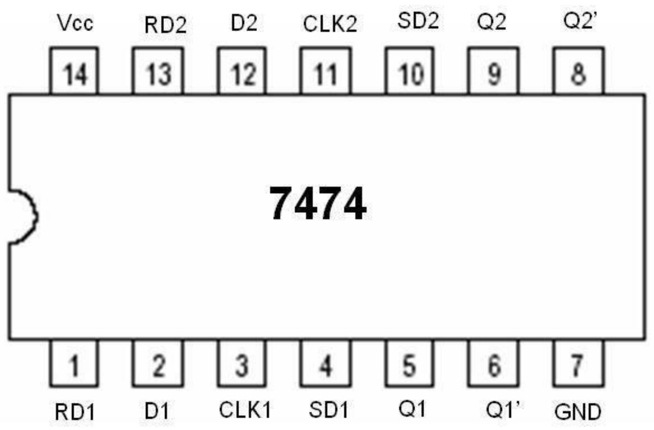
THEORY:

A pseudo random number generator (PRNG),also known as a deterministic random bit generator(DRBG), is an algorithm for generating a sequence of numbers whose properties approximate the properties of sequences of random numbers. The PRNG-generated sequence is not truly random, because it is completely determined by an initial value, called the PRNG's seed (which may include truly random values). Although sequences that are closer to truly random can be generated using hardware random number generators, pseudo random number generators are important in practice for their speed in number generation and the irreproducibility.

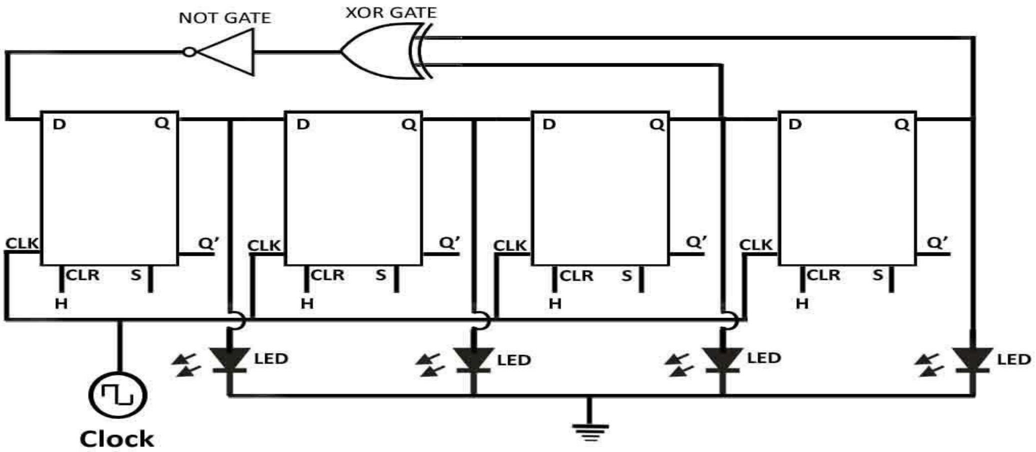
PRNGs are central in applications such as simulations(e.g. for the Monte Carlo method), electronic games(e.g. for procedural generation), and cryptography. Cryptographic applications require the output not to be predictable from earlier outputs, and more elaborate algorithms, which do not inherit the linearity of simpler PRNGs, are needed.

Good statistical properties area central requirement for the output of a PRNG. In general, careful mathematical analysis is required to have any confidence that a PRNG generates numbers that are sufficiently close to random to suit the intended use. John von Neumann cautioned about the misinterpretation of a PRNG as a truly random generator, and joked that "Anyone who considers arithmetical methods of producing random digits.

PIN CONFIGURATION:



CIRCUIT DIAGRAM:



PROCEDURE:

1. Connect the circuit as show in the circuit diagram.
2. Connect the NOT Gate to the D terminal and another terminal to XOR Gate as shown above in the diagram.
3. XOR Gate other to Q and LED and another terminal to Q and another LED as shown in above diagram.
4. Connect the Q to D as shown in above circuit.
5. Connect CLK O/P to CLK I/P terminals as shown.
6. Connect the all CLR to the Input Switch.
7. Observe the O/P which 4bit Pseudo random sequence using 4 bit ring counter.

TRUTH TABLE:

D	QA	QB	QC	QD
1	0	0	0	0
1	1	0	0	0
1	1	1	0	0
0	1	1	1	0
1	0	1	1	1
1	1	0	1	1
0	1	1	0	1
0	0	1	1	0
1	0	0	1	1
0	1	0	0	1
1	0	1	0	0
0	1	0	1	0
0	0	1	0	1
0	0	0	1	0

0	0	0	0	1
1	0	0	0	0

RESULT:

The Pseudo Random Sequence Generator using Ring Counter was constructed and studied.

VIVA QUESTIONS:

1. Pseudo Random Sequence Generator also known as what?
2. Ring counter belong to which type of counter?
3. What are the types of ring counter?
4. What is the difference between Johnson Ring Counter and synchronous ring counter?
5. What is meant by pseudo random number generator?
6. List out the applications of PRNG.
7. TRNG stands for
8. Define Uniformity in PRNG
9. Define scalability.
10. Why PRNGs are derived through algorithms.
11. What are the differences between half adder and full adder?
12. What are the advantages of minimizing the logical expressions?
13. What does a combinational circuit mean?
14. What is the difference between sequential and combinational circuit?
15. What is a flip-flop?. Explain the functions of preset and clear inputs in flip- flop?
16. What is meant by a clocked flip-flop?
17. What is meant by excitation table?
18. What is the difference between flip-flop and latch?
19. What are the various methods used for triggering flip-flops?
20. Explain level triggered flip-flop?
21. Explain the operation of IC 74X93?
22. Write the syntax for component instantiation?
23. What is net list?
24. Briefly explain about generics?
25. Write the difference between sequential statement and concurrent statement?
26. Write the syntax for loop statements?
27. Write the syntax for generate statements?

28. Write the differences between loop and generate?
29. What does priority encoder mean?7.
30. How many decoders are needed to construct 4X16 decoder?
31. List out the applications of PRNG.
32. TRNG stands for
33. Define Uniformity in PRNG
34. Define scalability.
35. Write the syntax for component declaration.
36. Write the behavioral code for IC 74x189 without declaring the function
37. Explain about different types of RAMs?
38. How to specify the memory size?
39. Explain read and write operations
40. List the different types of shift registers?
41. What is Magnitude Comparator?
42. List out the applications of comparators?
43. What is digital comparator?
44. Realize a single bit comparator?
45. Which logic gate is a basic comparator?
46. When are two numbers are equal?
47. What are the different types of comparator?
48. What are the advantages of comparator?
49. If two numbers are not equal then binary variable will be
50. What are synchronous counters?

EXPERIMENT-11

16x1 MULTIPLEXER USING TWO 8x1 MULTIPLEXERS

AIM:
To verify the truth table of 16x1 Multiplexer using Two 8x1 Multiplexer.

APPARATUS:
1. 16x1 Multiplexer using Two 8x1 Multiplexer.
2. Connecting Wires.

THEORY:
Multiplexer is one of the basic building units of a computer system which in principle allows sharing of a common line by more than one input lines. It connects multiple input lines to a single output line. At a specific time one of the input lines is selected and the selected input is passed on to the output line.

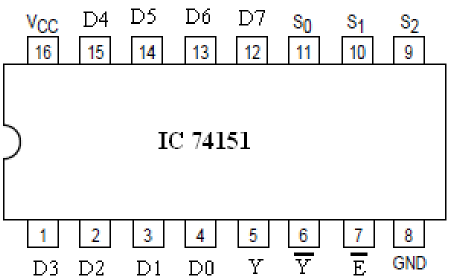
Relation between multiple Input lines and Selection lines

Input lines 16 $=2^4$i.e.4Seletion lines

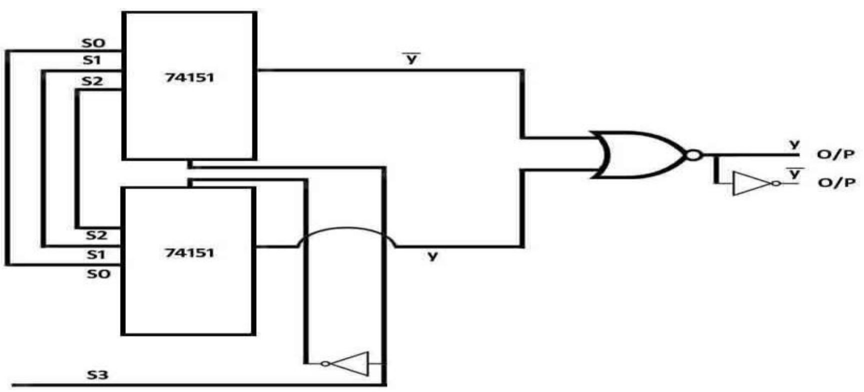
Input lines will be I0- I15

Selection lines will be S0-S3

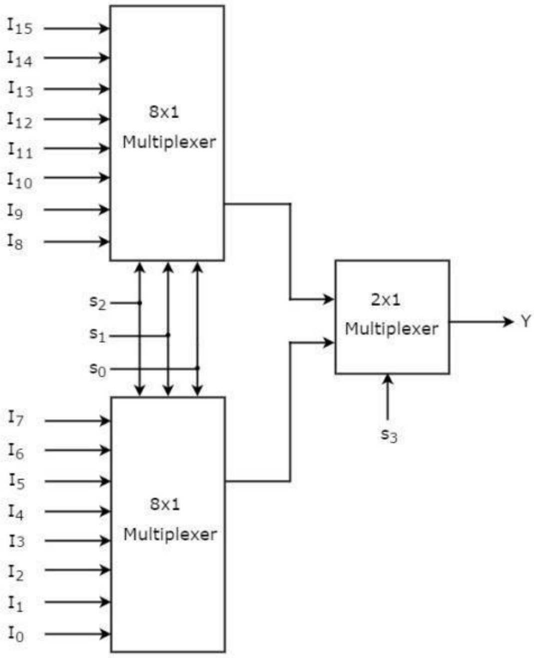
PIN CONFIGURATION:



CIRCUIT DIAGRAM:
Circuit Diagram using Gates:



Circuit Diagram using IC74157(2x1 Mux):



The diagram will be same as of the block diagram of 16-to-1 line multiplexer in which 8-to-1 line multiplexer Selection lines will be S0-S2 and S3 will be connected to 2-to-1 line multiplexer Selection and First 8-to-1 line multiplexer Input lines will be I0 -I7 and Second 8-to-1 line multiplexer Input lines will be I8 -I15. Let us implement 16x1 Multiplexer using 8x1 Multiplexers and 2x1 Multiplexer. We know that 8x1 Multiplexer has 8 data inputs, 3 selection lines and one output. Whereas, 16x1 Multiplexer has 16 data inputs, 4 selection lines and one output. So, we require two 8x1 Multiplexers in first stage in order to get the 16 data inputs. Since, each 8x1 Multiplexer produces one output, we require a 2x1 Multiplexer in second stage by considering the outputs of first stage as inputs and to produce the final output. Let the 16x1 Multiplexer has sixteen data inputs I15 to I0, four selection lines s3 to s0 and one output Y. The Truth table of 16x1 Multiplexer is shown below. The same selection lines, s2, s1 & s0 are applied to both 8x1 Multiplexers. The data inputs of upper 8x1 Multiplexer are I15 to I8 and the data inputs of lower 8x1 Multiplexer are I7 to I0. Therefore, each 8x1 Multiplexer produces an output based on the values of selection lines, s2, s1 & s0. The outputs of first stage 8x1 Multiplexers are applied as inputs of 2x1 Multiplexer that is present in the second stage. The other selection line, s3 is applied to 2x1 Multiplexer.

- If s3 is zero, then the output of 2x1 Multiplexer will be one of the 8 inputs Is 7 to I0 based on the values of selection lines s2, s1&s0.
- If s3 is one, then the output of 2x1 Multiplexer will be one of the 8 inputs I15 to I8 based on the values of selection lines s2, s1& s0. Therefore, the overall combination of two 8x1 Multiplexers and one 2x1 Multiplexer performs as one 16x1 Multiplexer.

PROCEDURE:

1. Connect the input as shown in the Truth Table to the logic switches which are provided on the trainer board.
2. Connect the output to the LED’s switch are provided on the trainer board.
3. Connect the **S3, S2, S1, S0** Inputs from the outputs provided on the trainer board.
4. Switch ON the trainer kit.

5. Note down the output and compare with the truth table.

TRUTH TABLE:

Selection Inputs				Output
S3	S2	S1	S0	Y
0	0	0	0	I0
0	0	0	1	I1
0	0	1	0	I2
0	0	1	1	I3
0	1	0	0	I4
0	1	0	1	I5
0	1	1	0	I6
0	1	1	1	I7
1	0	0	0	I8
1	0	0	1	I9
1	0	1	0	I10
1	0	1	1	I11
1	1	0	0	I12
1	1	0	1	I13
1	1	1	0	I14
1	1	1	1	I15

RESULT:

The truth table of 16x1 Multiplexer using Two 8x1 Multiplexer was verified.

VIVA QUESTIONS

1. What is a multiplexer?
2. Which combinational circuit is renowned for selecting a single input from multiple inputs & directing the binary information to output line?
3. Which is the major functioning responsibility of the multiplexing combinational circuit?
4. How many select lines would be required for an 8-line-to-1-line multiplexer?
5. How many NOT gates are required for the construction of a 4-to-1 multiplexer?
6. What are the applications of multiplexer and de-multiplexer?
7. In 2n to 1 multiplexer how many selection lines are there?
8. How to get higher order multiplexers?
9. Implement an 8:1 mux using 4:1 MUXS
10. What is the difference between multiplexer & demultiplexer?
11. Explain the operation of a digital multiplexer?
12. What makes the circuit of a multiplexer more complex?
13. What Is data selector?
14. What is a multiplexer?
15. Which mux without any additional circuitry can be used to obtain all the functions of 3 variable but not

all of 4 variables?

16. How many 2*1 mux are required to realize 4*1 mux and explain how?
17. Design a 4*1 mux using 2*1 mux?
18. What are the minimum number of 21 mux required to generate 2 input nandgate and a 2 input Ex-OR gate?
19. How a multiplexer can act as a universal combinational circuit explain?
20. Construct a NOT gate using 2*1 mux
21. . Construct a AND gate using 2*1 mux
22. Construct OR gate using 2*1 mux with n-1 selection lines
23. Construct a NAND gate using 2*1 mux
24. Construct a NOR gate using 2*1 mux
25. Construct a Ex-OR gate using 2*1 mux
26. Construct a Ex-NOR gate using 2*1 mux
27. How many 2*1 mux are required for 8*1 mux construction?
28. How many 2*1 mux are required for 16*1 mux construction?
29. How many 2*1 mux are required for 64*1 mux construction?
30. Obtain the logic for the construction of different multiplexers using 2*1 mux?
31. How can you classify different digital multiplexers?
32. What is synchronous multiplexer?
33. What is asynchronous multiplexer?
34. What is quasi-synchronous multiplexer?
35. What are advantages of digital multiplexing?
36. Will multiplexing create additional harmonics in the system?
37. What are the two basic multiplexing techniques?
38. Why are generally multiplexers are used?
39. What is demultiplexer?
40. What are the differences between multiplexer and demultiplexer?
41. How to get higher order multiplexers?
42. What are the different logic gates that are used in multiplexers? Draw their symbols?
43. What is data distributor?
44. How many data inputs does a mux have?
45. What are the components of a mux?
46. What is a combinational circuit?
47. Hat is the IC used in the design of 16*1 mux using two 8*1 mux?
48. What is an integrated circuit?

49. Draw the pin configuration of IC74151
50. How many selection lines are required for 8*1 mux?

EXPERIMENT-12

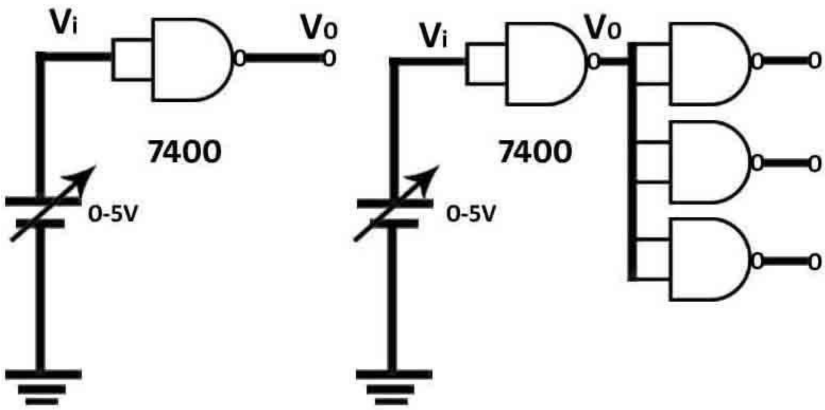
TRANSFORM CHARACTERISTICS OF 74H, LS, HS IC SERIES

AIM:
To plot a transform characteristic of 74H, LS and HS IC series.

APPARATUS:

1. Transform characteristics of 74H, LS a 74HS IC series trainer kit.
2. Patch cords.
3. Multimeter
4. CRO.

CIRCUIT DIAGRAM:



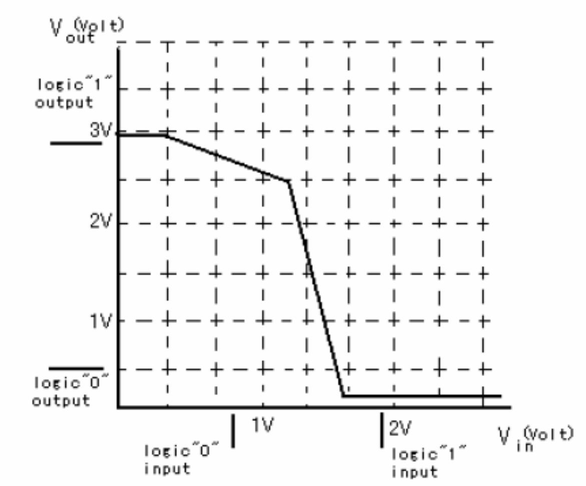
PROCEDURE:

1. Insert 74LS, 74HC,and74 HS any one IC in Socket as given on the trainer board to plot the characteristics.
2. Above circuit diagram given for the IC7400.
3. Connect the circuit as shown above.
4. Connect the Multimeter to Vi and Connect the Voltmeter to the Vo.
5. By varying the input voltage plot a graph between Input and Output.
6. Repeat the same procedure for different IC's.

Voltage Characteristics

1. If using an analog scope, connect the equipment and the component as shown below. If using a digital scope, connect the function generator to channel 1 and the device to channel 2 (opposite of diagram). Make sure both the function generator and the oscilloscope have the same ground.

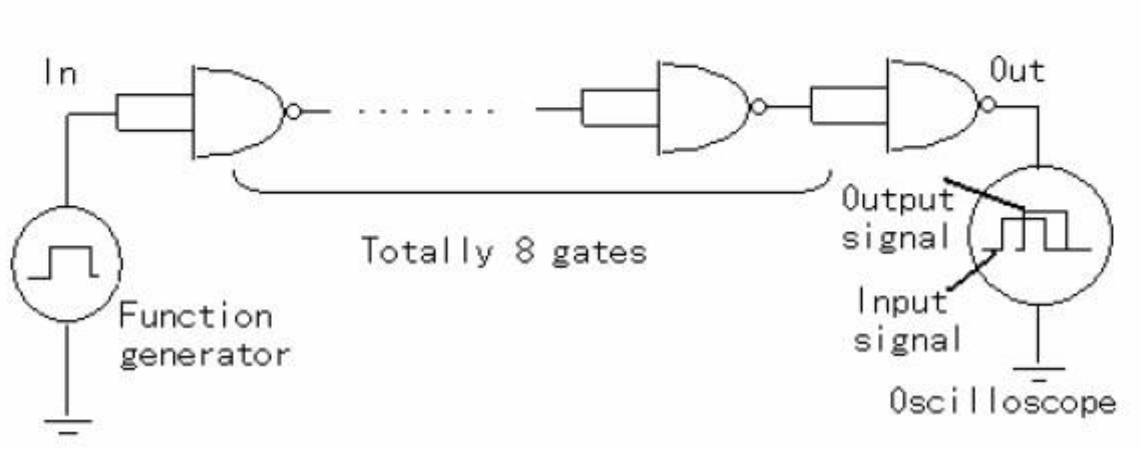
2. For the function generator,selecta0to5V sine wave with a frequency of 1kHz. For the oscilloscope, select the X-Y mode of operation. A trace similar to the one shown below should be obtained. This is called the transfer characteristic of the gate. Note that the input voltage, Vin, is on The X axis and the output voltage, Vout , on the Y axis.



Propagation Delay

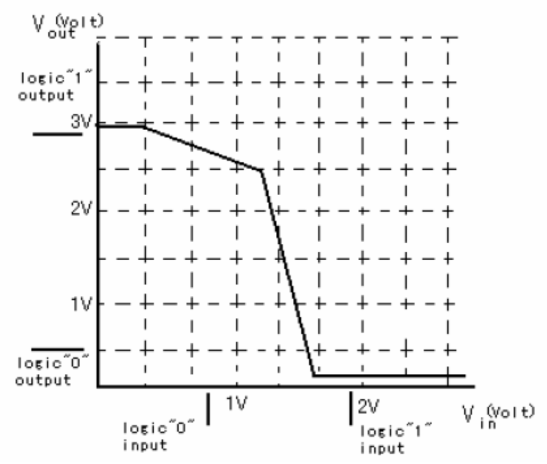
1. Using two 4011 chips, construct the circuits how n below. Use a chain of 8 gates(n=8) to determine the propagation delay tP. In order to obtain a good measurement of the delay time, a frequency of operation should be chosen sufficiently high so that the total delay in the chain(ntP)is comparable to the period of the input clock. Obtain the delay times tPHL and tPLH from the datasheets. Use The oscilloscope to measure Vin and Vout. Use a squarewave as input.

   Why can we not measure both tPHL and tPLH from the circuit shown? [Hint: how many gates do we have and what is the relationship between the input and the output?]



2. The propagation delay of a CMOS gate is a function of the load capacitance and the supply voltage VDD. Determine the propagation delay tP as a function of VDD. Use a variable power supply and measure with VDD at 5V, 10V, and 15V.

EXPECTED GRAPH:



RESULT:

The transform characteristics of 74H, LS and HS IC series was plotted.

VIVA QUESTIONS:

1. Define propagation delay
2. Define rise time.
3. What is Boolean Algebra?
4. Define a logic-gate. Why is it called so?
5. What is positive logic and negative logic?
6. Define a truth table.
7. Define an analog signal and a digital signal.
8. List out the ICs for various logic operations like NAND, NOR, XOR, OR, AND etc.
9. What is De Morgan's theorem?
10. What is the use of De Morgan's theorem?
11. Implement the various logics using the NOR gate.
12. Implement the various logic gates using the NAND gate.
13. What is an integrated circuit?
14. What are the different categories of IC's?
15. What is LS in 74LS IC?
16. Which IC's among 74LS 74HC & HS are static sensitive?
17. What is the use of De Morgan's theorem?

18. Implement various logics using NAND gate?
19. Implement various logics using NOR gate?
20. What is the drawback of ICs?
21. Why are ICs so cheap?
22. Why do ICs need small power for their operation?
23. What are the advantages of IC over discrete components?
24. Why are ICs more reliable?
25. What are the important IC technologies used?
26. What is a monolithic IC?
27. Why is sio2 layer formed over the entire surface in a monolithic IC?
28. How is sio2 layer formed in a monolithic IC?
29. In IC’s the substrate is not employed as collector why?
30. Why is the diffusion technique of formation of resistor most widely used?
31. Why is the plastic DIP IC package most widely used?
32. With what material are ICs generally made?
33. What is the most popular package of IC?
34. What are the elements that cannot be fabricated on IC?
35. What are the types of IC’s?
36. Write the examples of linear IC’s?
37. What are the examples of Digital IC’s?
38. Audio amplifier is an example of which IC?
39. What are the active and passive elements?
40. What are the active components in IC?
41. Is sio2 layer of IC an insulating layer or a resistor? Explain
42. Define propagation delay?
43. Define rise time?
44. What is Boolean algebra?
45. Define logic gate and why is it called so?
46. What is positive logic and negative logic?
47. Define truth table.
48. Define an analog signal and a digital signal?
49. List out the IC’s for various operations like NAND NOR XOR AND NOTetc
50. What is De Morgan’s theorem?

EXPERIMENT-13

4 BIT GRAY TO BINARY AND BINARY TO GRAY CONVERTER

AIM:

To Convert 4 Bit Gray to Binary and Binary to Gray

APPARATUS:

1. 4 Bit Gray to Binary and Binary to Gray Converter Trainer kit.
2. Connecting Wires.

THEORY:

Binary-to-Gray Converter: An interesting application for the exclusive-OR gate is a logic gate to change a binary number to its equivalent in Gray Code. The logic circuit can be used to convert a 4-bit binary number ABCD into its Gray-code equivalent, G1, G2, G3, and G4. As an example, the binary number 0011 will be converted into its Gray-Code equivalent of 0010 by the circuit. Note: A is the most significant bit and D is the least significant bit.

The availability of a large variety of codes for the same discrete elements of information results in the use of different codes by different digital systems. It is sometimes necessary to use the output of one system as the input to another. A conversion circuit must be inserted between the two systems if each uses different codes for the same information. Thus, a code converter is a circuit that makes the two systems compatible even though each uses a different binary code.

The binary number system is a system that uses only the digits 0 & 1 as codes. To represent a group of 2^n distinct elements in a binary code requires a minimum of n bits. This is because it is possible to arrange bits in 2^n distinct ways. Although the minimum number of bits required to code 2^n distinct quantities is n, there is no maximum number of bits that may be used for binary code. For example, a group of four distinct quantities can be represented by a two-bit code, with each quantity assigned one of the following bit combinations: 00, 01, 10, and 11. A group of eight elements requires a three-bit code, with each element assigned to one and only one of the following 000, 001, 010, 011, 100, 101, 110, and 111.

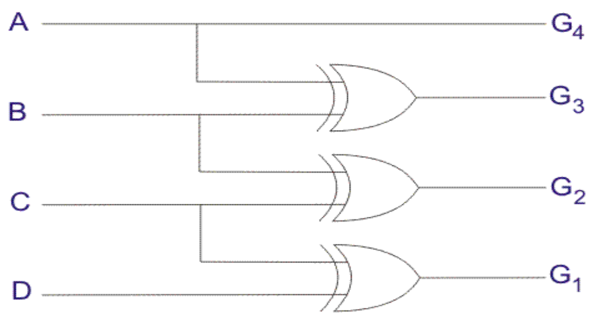
Gray code (reflected code). Number in the gray code changes by only one bit as it proceeds from one number to the next. For example, in going from decimal 7 to 8, the gray code number changes from 0100 to 1100; these numbers differ only in MSB. So it is with the entire gray code; every number differs by only one bit from the preceding number. The logic diagram for binary code to gray code converter and gray code to binary code converter.

The logic equations for

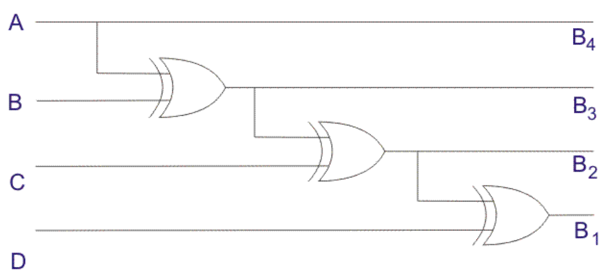
Binary to gray code

conversion G0= B0 ÅB1
G1 =B1ÅB2
G2 =B2ÅB3
G3 =B3
Gray to binary code
conversion B0 =G3ÅG2Å G1
ÅG0
B1= G3 ÅG2 Å
G1B2 =G3ÅG2
B3= G3

CIRCUIT DIAGRAM:



Logic Circuit for Binary to Gray Code Converter



Logic Circuit for Gray to Binary Code Converter

PROCEDURE:

Gray to Binary converter:

1. Connect the A, B, C, and D to the Input switches.
2. Connect the B4, B3, B2, and B1to the Output LED's.
3. Verify the Gray to Binary conversion by following truth table.

Binary to Gray converter:

1. Connect the A, B, C, and D to the Input switches.
2. Connect the G4, G3, G2, and G1 to the Output LED's.
3. Verify the Binary to Gray conversion by following truth table.

TRUTH TABLE:

Binary to Gray conversion:

Decimal Number	4BitBinaryNumber **ABCD**	4BitGrayCode **G1G2G3G4**
0	0000	0000
1	0001	0001
2	0010	0011
3	0011	0010
4	0100	0110
5	0101	0111
6	0110	0101
7	0111	0100
8	1000	1100
9	1001	1101
10	1010	1111
11	1011	1110
12	1100	1010
13	1101	1011
14	1110	1001
15	1111	1000

Gray to Binary to Conversion:

4 Bit Gray Code	4 Bit Binary Code
0000	0000
0001	0001
0011	0010
0010	0011
0110	0100
0111	0101
0101	0110
0100	0111
1100	1000
1101	1001
1111	1010
1110	1011
1010	1100
1011	1101
1001	1110
1000	1111

RESULT:

The 4 Bit Gray to Binary and Binary to Gray was converted and the results are verified.

VIVA QUESTIONS:

1. What is gray code?
2. A code converter is a logic circuit that?
3. Reflected binary code is also known as?
4. Why do we use gray codes?
5. Convert binary number into gray code: 100101
6. The primary use for gray code is
7. Code is a symbolic representation of?
8. Why is the gray code more practical to use when coding the position of a rotating shaft?
9. If two numbers are not equal then binary variable will be?
10. 74ls85 is a?
11. What is a code converter?

12. What is the use of gray code?
13. What is the code?
14. What is the other name for gray code?
15. Why is the gray code more practical to use when coding the position of a rotating shaft?
16. Why do we use gray codes?
17. One way to convert bcd to binary using the hardware approach is?
18. Earlier, reflected binary codes were applied to?
19. Convert binary number into gray code: 100101
20. The binary representation of bcd number 00101001
21. Gray code representation of 14 is
22. 01001101 represents the letter m in
23. How many bits are in a byte?
24. Convert hexadecimal value 16 to decimal.
25. Are the voltages in digital electronics are continuously variable?
26. Which is typically the longest: bit, byte, nibble, word?
27. Convert the binary number 1100 to gray code.
28. Convert the gray code 1011 to binary.
29. What is the difference between binary coding and binary-coded decimal?
30. Digital electronics is based on the which numbering system.
31. The 1's complement of 10011101 is
32. An informational signal that makes use of binary digits is considered to be:
33. The binary-coded decimal (bcd) system can be used to represent each of the 10 decimal digits as which code?
34. The decimal number 18 is equal to which binary number?
35. A code converter is a logic circuit that?
36. Reflected binary code is also known as?
37. The primary use of gray code is?
38. Code is a symbolic representation of?
39. If two numbers are not equal then their binary variable will be?
40. Ttl74ls85 is a?
41. What is the function of an enable input on a multiplexer chip?
42. How many outputs are on a bcd decoder?
43. What is an encoder?

44. What is a decoder?
45. In a gray code, each number is 3 greater than the binary representation of that number is it true or false justify?
46. Use the weighting factors to convert the following bcd numbers to binary.
47. 0101 0011 0010 0110 1000
48. Which digital system translates coded characters into a more useful form?
49. How many inputs will a decimal-to-bcd encoder have?
50. A principle regarding most ic decoders is that when the correct input is present, the related output will switch:

EXPERIMENT-14

RING COUNTER & TWISTED RING COUNTER USING 4BIT SHIFT REGISTER

AIM:

To Construct a Ring Counter and Twisted Ring Counter using 4Bit Shift Register.

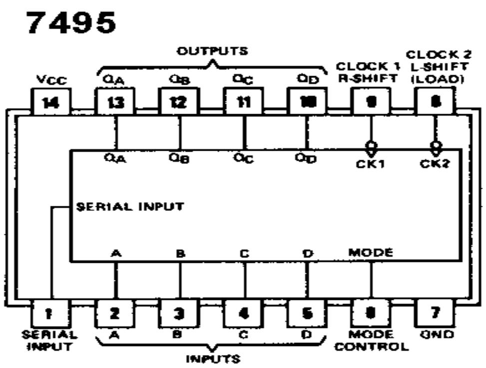
APPARATUS:

1. Ring Counter and Twisted Ring Counter using Bit Shift Register Trainer kit.
2. Patch Cords.

THEORY:

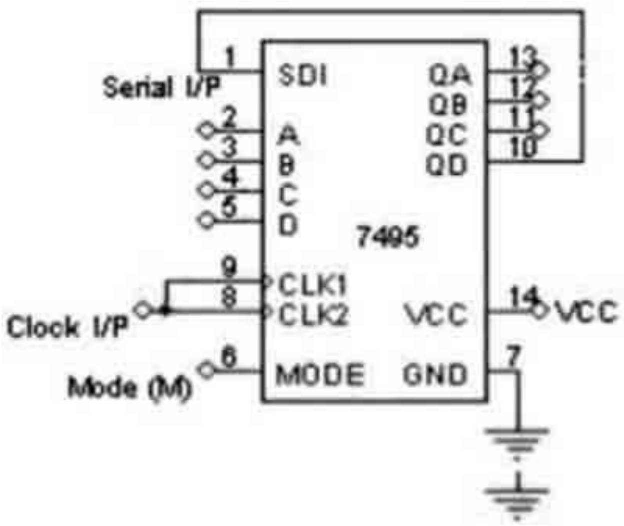
Ring counter is a basic register with direct feedback such that the contents of the register simply circulate around the register when the clock is running. Here, the last output that is QD in a shift register is connected back to the serial input. A basic ring counter can be slightly modified to produce another type of shift register counter called Johnson counter. Here, complement of last output is connected back to the not gate input and not gate output is connected back to serial input. A four-bit Johnson counter gives 8 state output.

PIN CONFIGURATION:

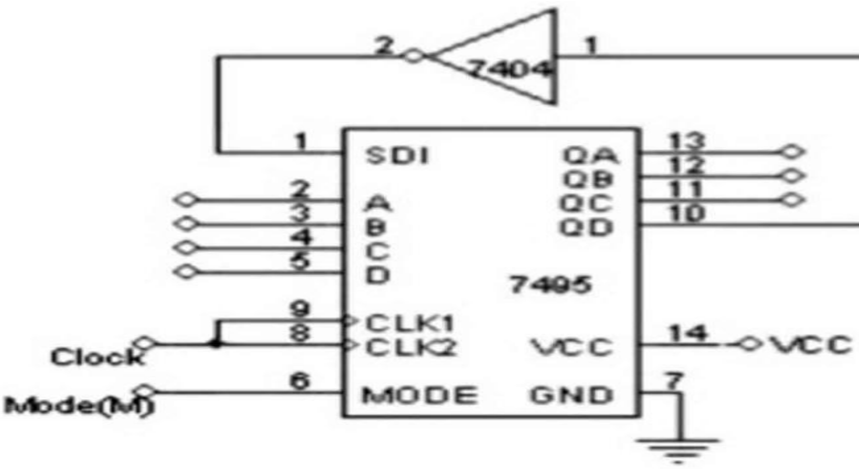


CIRCUIT DIAGRAM:

Ring Counter:



Twisted Ring Counter:



PROCEDURE:

Ring Counter:

1. Make the Connection as show in the Ring Counter Circuit Diagram.
2. Connect Inputs A, B, C, D to input switch present on trainer kit.
3. Connect the Outputs QA, QB, QC, QD
4. Connect the Serial I/P to Pin10 of the 7495IC i.e., QD
5. Connect 8th and 9th Pins of the IC79 to Clock, which is present on the trainer.
6. Connect Mode 6th Pin of IC7495 to Input Switch
7. Verify the truth table of Ring counter.

Twisted Ring Counter:

1. Make the Connection as show in the Twisted Ring Counter Circuit Diagram.
2. Connect Inputs A, B, C, D to input switch present on trainer kit.
3. Connect the Outputs QA, QB, QC, QD.
4. Connect the Serial I/P to NOT Gate, which is present on trainer kit
5. Connect another terminal of the NOT Gate to Pin10 of the7495IC i.e., QD
6. Connect 8th and 9th Pins of the IC7495 to Clock, which is present on the trainer.
7. Connect Mode 6th Pin of IC7495 to Input Switch
8. Verify the truth table of Twisted Ring counter

TRUTH TABLE:

Ring Counter:

Set the Mode to High and Low condition for reset.

Clock	QA	QB	QC	QD
0	1	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	0	0	1
4	1	0	0	0
5	0	1	0	0
6	0	0	1	0
7	0	0	0	1
8	1	0	0	0

Twisted Ring Counter:

Clock	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1
8	0	0	0	0

Results

A Ring Counter and Twisted Ring Counter using 4Bit Shift Register was constructed and implemented.

VIVA QUESTIONS

1. Define Ring counter?
2. By adding recirculation lines to a 4-bit parallel-in serial-out shift register, it becomes a ________, ________, and ________out register.
3. What type of register would have a complete binary number shifted in one bit at a time and have all the stored bits shifted out one at a time?
4. When is it important to use a three-state buffer?

5. A bidirectional 4-bit shift register is storing the nibble 1110. Its input is LOW. The nibble 0111 is waiting to be entered on the serial data-input line. After two clock pulses, the shift register is storing ________
6. In a parallel in/parallel out shift register, D0 = 1, D1 = 1, D2 = 1, and D3 = 0. After three clock pulses, the data outputs are ________
7. The group of bits 10110111 is serially shifted (right-most bit first) into an 8-bit parallel output shift register with an initial state 11110000. After two clock pulses, the register contains
8. What type of register would have a complete binary number shifted in one bit at a time and have all the stored bits shifted out one at a time?
9. In a 4-bit Johnson counter sequence there are a total of how many states, or bit patterns?
10. If a 10-bit ring counter has an initial state 1101000000, what is the state after the second clock pulse?
11. How much storage capacity does each stage in a shift register represent?
12. Ring shift and Johnson counters are-----------
13. What is the difference between a shift-right register and a shift-left register?
14. What is a transceiver circuit?
15. A 74HC195 4-bit parallel access shift register can be used for………………. operation
16. Which type of device may be used to interface a parallel data format with external equipment's serial format?
17. What is the function of a buffer circuit?
18. What is the preset condition for a ring shift counter?
19. Which is not characteristic of a shift register?
20. To keep output data accurate, 4-bit series-in, parallel-out shift registers employ a------------
21. Another way to connect devices to a shared data bus is to use a…………..
22. A down counter using n-flip-flops count……………….
23. UP Counter is…………………
24. DOWN counter is…………………
25. How many different states does a 3-bit asynchronous down counter have?...................
26. In a down counter, which flip-flop doesn't toggle when the inverted output of the preceeding flip-flop goes from HIGH to LOW.
27. In a 3-bit asynchronous down counter, the initial content is
28. In a 3-bit asynchronous down counter, at the first negative transition of the clock, the counter content becomes
29. In a 3-bit asynchronous down counter, at the first negative transition of the clock, the counter content becomes
30. The hexadecimal equivalent of 15,536 is ________
31. Define static RAM

32. Define dynamic RAM
33. Classify types of ROMs
34. Applications of ROMS
35. What is the difference between latch & Flip-Flop, Explain with logic diagram?
36. Explain any one application of SR latch.
37. What is race around condition? How it is avoided?
38. How synchronous counters differ from asynchronous counters?
39. List counter applications.
40. State various applications of counters.
41. Difference between Asynchronous clock and Synchronous Clock
42. Draw the truth table of SR and JK
43. Draw the Excitation Table of SR and JK
44. Give the Excitation Table of D and T Flip Flop
45. What is meant of Edge Triggering?
46. Types Of Shift Registers.
47. Specify the operations done on Shift Registers
48. Explain the decade counter
49. Draw the Logic diagram for Conversion of D-SR
50. List the Counter Types

EXPERIMENT-15

4 DIGITS HEX COUNTER USING SYNCHRONOUS ONE DIGIT HEX COUNTERS

AIM:
To Construct a 4 Digit Hex Counter using 1 Digit synchronous Hex counter.

APPARATUS:
1. Digit Hex counter using 1 Digit Synchronous Hex counter.
2. Patch Cords

THEORY:

When working with large digital systems, such as computers, it is common to find binary numbers consisting of 8, 16, and even 32 digits which makes it difficult to read and write without producing errors, especially when working with lots of 16 or 32-bit binary numbers.

One common way of overcoming this problem is to arrange the binary numbers into groups or sets of four bits (4-bits). These groups of 4-bits use another type of numbering system also commonly used in computer and digital systems called Hexadecimal Numbers.

The hexadecimal or simply HEX numbering system uses the Base of 16 system and are a popular choice for representing long binary values because their format is quite compact and much easier to understand compared to the long binary strings of I's and o's.

Being a Base-16 system, the hexadecimal numbering system therefore uses 16 (sixteen) different digits with a combination of numbers from 0 through to 15. In other words, there are 16 possible digit symbols.

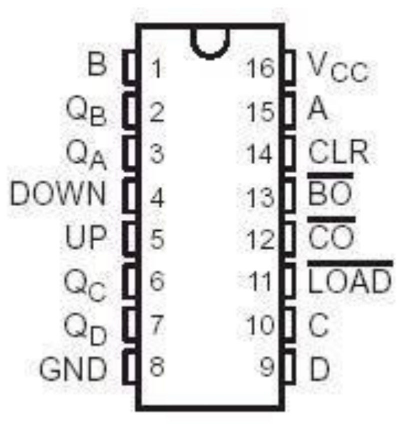
However, there is a potential problem with using this method of digit notation caused by the fact that the decimal numerals of 10, 11, 12, 13, 14 and 15 are normally written using two adjacent symbols. For example, if we write 10 in hexadecimal, do we mean the decimal number ten, or the binary number of two (1+0). To get around this tricky problem, hexadecimal numbers that identify the values of ten, eleven, ..., fifteen are replaced with capital letters of A, B, C, D, E, and F respectively. Then in the Hexadecimal Numbering System we use the numbers from 0 to 9 and the capital letters A to F to represent its Binary or Decimal number equivalent, starting with the least significant digit at the right-hand side. As we have just said, binary strings can be quite long and difficult to read, but we can make life easier by splitting these large binary numbers up into even groups to make them much easier to write down and understand. For example, the following group of binary digits 1101 0101 1100 1111 2 are much easier to read and understand than 11010101110011112 when they are all bunched up together. In the everyday use of the decimal numbering systems, we use groups of three digits or 000's from the right-hand side to make a very large number such as a million or trillion, easier for us to understand and the same is also true in digital systems. Hexadecimal Numbers is a more complex system than using just binary or decimal and is mainly used when dealing with computers and memory address locations. By dividing a binary number up into groups of 4 bits, each group of 4 digits can now have a possible value of between "0000" (0) and "1111" (8+4+2+1=15) giving a total of 16 different number combinations from 0 to 15, Don't forget that "0" is also a valid digit. We remember from our first tutorial about Binary Numbers that a 4-digit group of digits is called a "nibble" and as 4 bits are also required to produce a hexadecimal number, a hex digit can also be thought of as a nibble, or half-a-byte. Then two hexadecimal numbers are required to produce one full byte ranging from 00 to FF.

Also, since 16 in the decimal system is the fourth power of 2 (or 2^4), there is a direct relationship between the numbers 2 and 16, so one hex digit has a value equal to four binary digits, so now q is equal to "16".

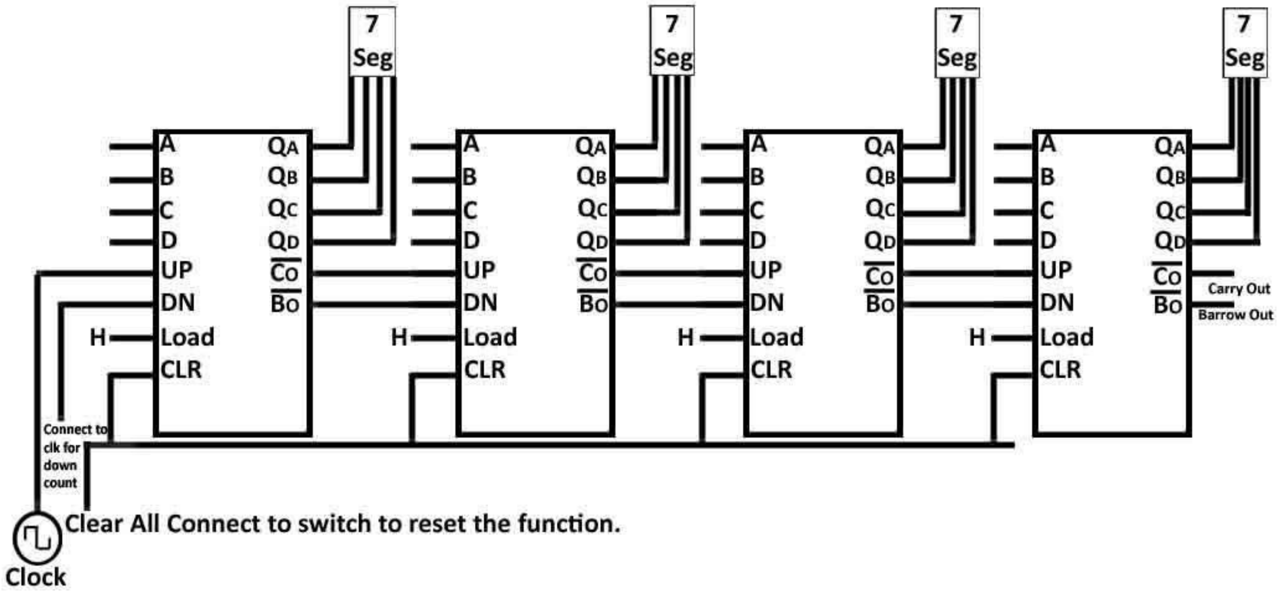
Because of this relationship, four digits in a binary number can be represented with a single hexadecimal digit. This makes conversion between binary and hexadecimal numbers very easy, and hexadecimal can be used to write large binary numbers with much fewer digits.

The numbers 0 to 9 are still used in the original decimal system, but the numbers from 10 to 15 are now represented by capital letters of the alphabet from A to F inclusive and the relationship between decimal, binary, and hexadecimal is given below.

PIN CONFIGRATION:



CIRCUIT DIAGRAM:



PROCEDURE:

1. Connect the circuit as shown in circuit diagram.
2. Connect UP of IC74193 to Clock I/P.
3. Connect Clear I/P's and connect to inputs switch, which are present on the trainer kit.
4. Connect QA, QB, QC, and Qd of all IC'stothe7 segment display.
5. Connect Carry out of IC74193 to UP terminal of other IC74193 as shown in the circuit diagram.
6. Observe Output according to the truth table.

TRUTH TABLE:

Decimal Number	4-bit Binary Number	Hexadecimal Number
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9

10	1010	A
11	1011	B
12	1100	C
13	1101	D
14	1110	E
15	1111	F
16	00010000	10(1+0)
17	00010001	11(1+1)

RESULT:

The 4 Digit Hex Counter using 1 Digit synchronous Hex counter was designed and implemented.

VIVA QUESTIONS:

1. State various applications of counters.
2. Difference between Asynchronous clock and Synchronous Clock
3. Draw the truth table of SR and JK
4. Draw the Excitation Table of SR and JK
5. Give the Excitation Table of D and T Flip Flop
6. What is meant of Edge Triggering?
7. Types Of Shift Registers.
8. Specify the operations done on Shift Registers
9. Explain the decade counter
10. Draw the Logic diagram for Conversion
11. A MOD-12 and a MOD-10 counter are cascaded. Determine the output frequency if the input clock frequency is 60 MHz
12. Which segments of a seven-segment display would be required to be active to display the decimal digit 2?
13. How many AND gates would be required to completely decode ALL the states of a MOD-64 counter, and how many inputs must each AND gate have?
14. A BCD counter is a ________.
15. How many flip-flops are required to construct a decade counter?
16. The terminal count of a typical modulus-10 binary counter is ________
17. A seven-segment, common-anode LED display is designed for……

18. How many flip-flops are required to make a MOD-32 binary counter?
19. Using four cascaded counters with a total of 16 bits, how many states must be deleted to achieve a modulus of 50,000?
20. A MOD-16 ripple counter is holding the count 1001_2. What will the count be after 31 clock pulses?
21. The terminal count of a modulus-11 binary counter is ________.
22. List which pins need to be connected together on a 7493 to make a MOD-12 counter.
23. How can a digital one-shot be implemented using HDL?
24. Integrated-circuit counter chips are used in numerous applications including…………
25. Synchronous construction reduces the delay time of a counter to the delay of:
26. Synchronous counters eliminate the delay problems encountered with asynchronous counters because the:
27. What is the difference between combinational logic and sequential logic?
28. What is the difference between a 7490 and a 7492?
29. When two counters are cascaded, the overall MOD number is equal to the ________ of their individual MOD numbers.
30. A MOD-12 and a MOD-10 counter are cascaded. Determine the output frequency if the input clock frequency is 60 MHz
31. Which segments of a seven-segment display would be required to be active to display the decimal digit 2?
32. How many AND gates would be required to completely decode ALL the states of a MOD-64 counter, and how many inputs must each AND gate have?
33. A BCD counter is a ________.
34. How many flip-flops are required to construct a decade counter?
35. The terminal count of a typical modulus-10 binary counter is ________.
36. A seven-segment, common-anode LED display is designed for………
37. Which of the following is an invalid output state for an 8421 BCD counter?
38. How many different states does a 3-bit asynchronous counter have?
39. A 5-bit asynchronous binary counter is made up of five flip-flops, each with a 12 ns propagation delay. The total propagation delay ($t_{p(tot)}$) is ________.
40. One of the major drawbacks to the use of asynchronous counters is: ------------------
41. Once an up-/down-counter begins its count sequence, it cannot be reversed. (True/False) ………….
42. Three cascaded modulus-5 counters have an overall modulus of ________.
43. An asynchronous 4-bit binary down counter changes from count 2 to count 3. How many

transitional states are required?

44. How many different states does a 3-bit asynchronous counter have?
45. A 5-bit asynchronous binary counter is made up of five flip-flops, each with a 12 ns propagation delay. The total propagation delay ($t_{p(tot)}$) is ________.
46. One of the major drawbacks to the use of asynchronous counters is: ------------------
47. Once an up-/down-counter begins its count sequence, it cannot be reversed. (True/False) …………..
48. Three cascaded modulus-5 counters have an overall modulus of ________.
49. An asynchronous 4-bit binary down
50. The final output of a modulus-8 counter occurs one time for every ________.

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EXPERIMENT-16

DESIGN OF 16×4 RAM USING 74189 IC AND STUDY OF READ/WRITE OPERATIONS

Aim:
To design a 16×4 RAM using 74189 IC and study its read and write operations.

Apparatus Required:

1. 74189 RAM IC,
2. breadboard, power supply (+5V),
3. connecting wires,
4. switches,
5. LEDs,
6. resistors.

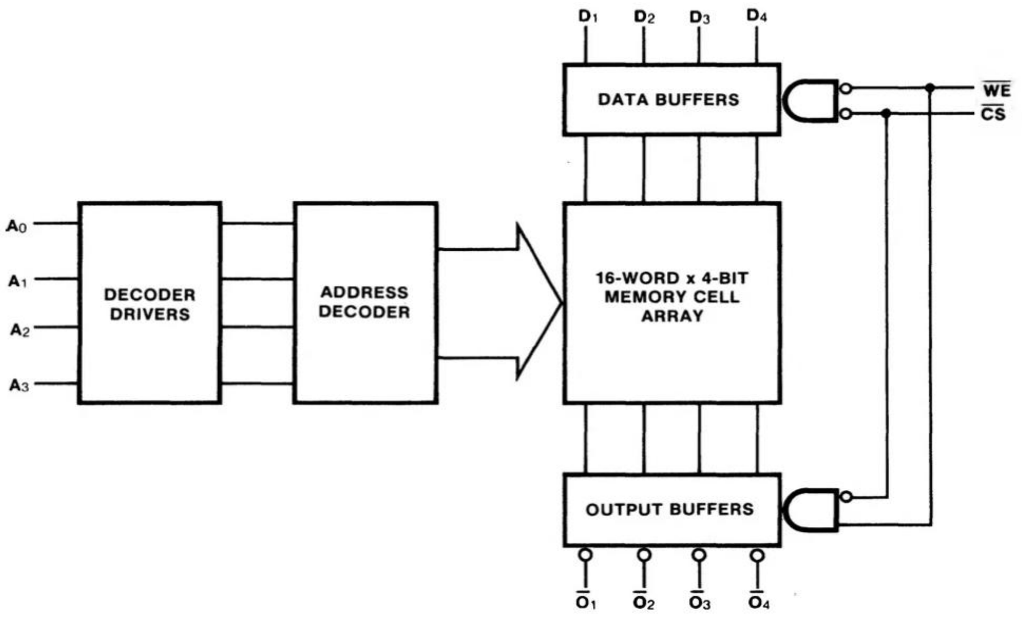
Theory:
The 74189 is a high-speed static RAM with a memory capacity of 16 words × 4 bits. It has 4 address lines (A0–A3) to select one of 16 memory locations. Data is stored in 4-bit words. The IC provides separate control for read and write operations. It has active low chip select and write enable signals. The outputs are typically inverted, so external inverters may be required depending on the application.

Pin Description (Important Signals):
A0–A3: Address inputs
D0–D3: Data inputs
O0–O3: Data outputs
$C\overline{S}$: Chip select (active low)
$W\overline{E}$: Write enable (active low)

Circuit Description:

- Connect A0–A3 to switches to select memory locations.
- Connect D0–D3 to input switches for entering data.
- Outputs O0–O3 are connected to LEDs (through resistors) to observe data.
- $C\overline{S}$ is grounded to enable the chip.
- $W\overline{E}$ is used to control read/write operation.

LOGIC DIAGRAM



Read/Write Operation:

Write Operation:

- Apply address on A0–A3.
- Apply data on D0–D3.
- Make $W\overline{E}$ = 0 (active low).
- Data is written into the selected memory location.

Read Operation:

- Apply address on A0–A3.
- Make $W\overline{E}$ = 1.
- Stored data appears at outputs O0–O3 (inverted form).

Truth Table:

$C\overline{S}$	$W\overline{E}$	Operation
0	0	Write
0	1	Read
1	X	Disabled

Procedure:

1. Make the circuit connections as per the design.
2. Switch ON the power supply.
3. Select a memory location using address inputs.
4. Apply input data through switches.
5. Perform write operation by making $W\overline{E}$ = 0.
6. Change $W\overline{E}$ = 1 to read the stored data.

7. Observe output on LEDs.
8. Repeat for different addresses and data values.

Result:
The 16×4 RAM was successfully designed using 74189 IC and read/write operations were verified.

VIVA QUESTIONS:
1. What is RAM?
2. What is the full form of RAM?
3. What is the function of memory in digital systems?
4. What is the difference between RAM and ROM?
5. What type of memory is 74189?
6. What is the memory capacity of 74189 IC?
7. What does 16×4 RAM mean?
8. How many address lines are required for 16 memory locations?
9. How many data bits are stored in each location of 74189?
10. What are the address inputs of 74189?
11. What are the data inputs of 74189?
12. What are the data outputs of 74189?
13. What is the function of chip select ($C\overline{S}$)?
14. Why is $C\overline{S}$ active low?
15. What is the function of write enable ($W\overline{E}$)?
16. What happens when $W\overline{E} = 0$?
17. What happens when $W\overline{E} = 1$?
18. What is the role of address lines?
19. How is a memory location selected?
20. What is the difference between read and write operations?
21. What is meant by volatile memory?
22. Is 74189 volatile or non-volatile?
23. Why is RAM called read/write memory?
24. What is the significance of active low signals?
25. What happens when $C\overline{S} = 1$?
26. Why are outputs of 74189 inverted?
27. How can inverted outputs be corrected?
28. What is propagation delay in RAM?
29. What is access time of memory?
30. What is the importance of access time?
31. What type of RAM is 74189 (static or dynamic)?

32. What is static RAM?
33. What is dynamic RAM?
34. Why is SRAM faster than DRAM?
35. What are the advantages of SRAM?
36. What are the disadvantages of SRAM?
37. How many memory locations are present in 74189?
38. What is meant by word length?
39. What is the function of LEDs in the experiment?
40. Why are resistors used with LEDs?
41. What is the purpose of a breadboard?
42. What is meant by memory decoding?
43. Can we expand memory capacity using multiple ICs?
44. How can you design a larger RAM using 74189 ICs?
45. What is the power supply required for 74189?
46. What will happen if power supply is removed?
47. What is data retention in RAM?
48. What are the applications of RAM?
49. What is meant by memory organization?
50. Why is RAM important in microprocessor systems?